

# MEMS-CMOS Integration and Beyond

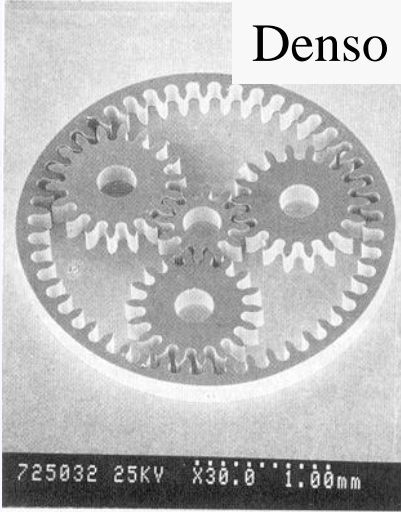
Hiroyuki Fujita, Agnes-Tixier Mita, Hiroshi Toshiyoshi  
Center for International Research on Micronano  
Mechatronics  
IIS, The University of Tokyo

# Content

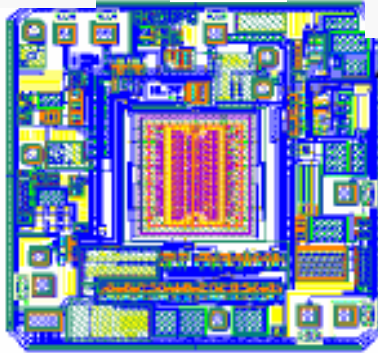
- MEMS trend toward MEMS-CMOS integration
- Examples of MEMS-CMOS integration
- Beyond MEMS-CMOS integration

# Examples of MEMS devices

Denso



AD

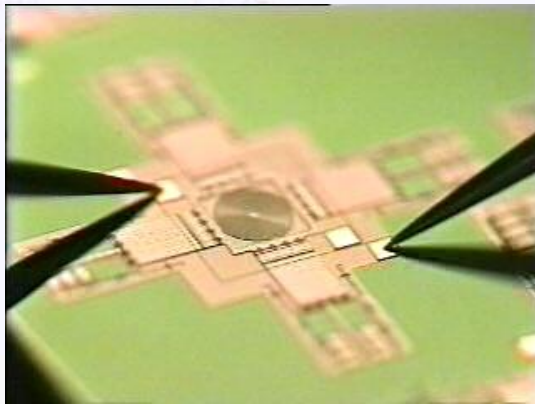
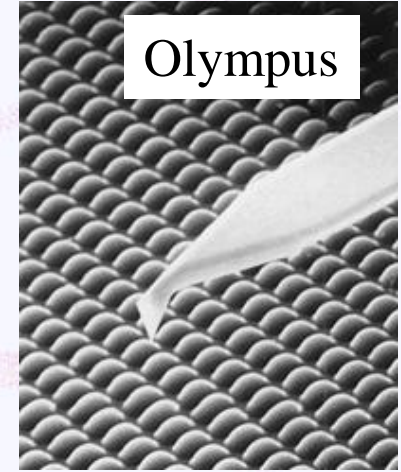


XL150  
New

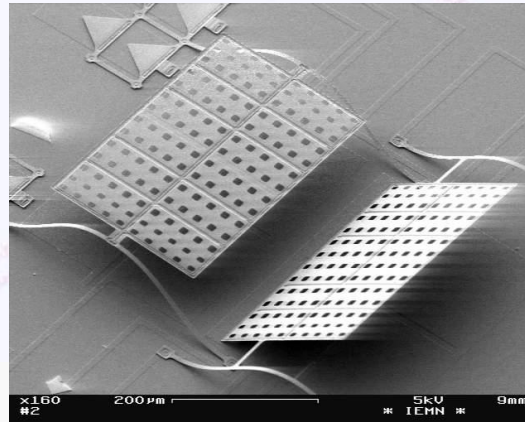
U-Tokyo



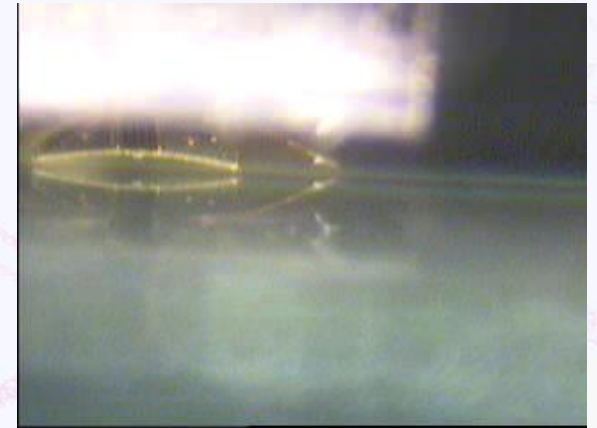
Olympus



UC Berkeley



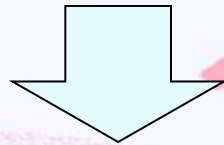
IEMN/CNRS



Northeastern Univ.

# MEMS Development in Last Decade

- Almost all the important processes and devices in micro-scale already existed 10 years ago, e.g. DRIE, bonding, microactuators, etc.



- **Technological sophistication,**
- **Application diversity** increase
- **Performance** improvement.
- **Commercial products** have flourished.



# Now MEMS is everywhere around you, and even more in the future.

- In your car
- In your camera
- In your smart phone
- In your TV game controller
- In your video projector
- In your printer
- In your computer
- In your (?) robot

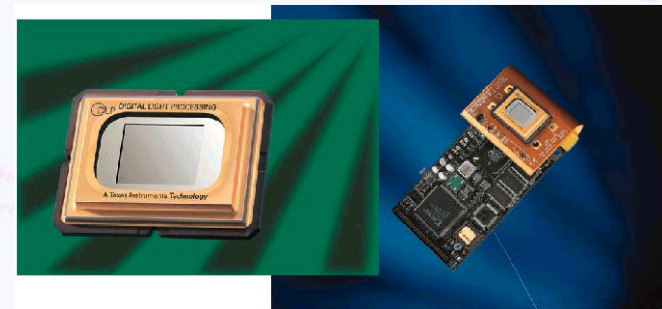


Nintendo Wii™ controller

Apple  
iPhone



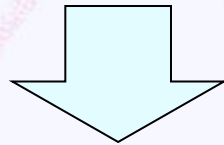
Honda Asimo



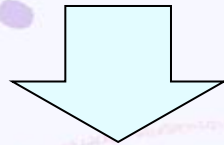
Digital Light Processing™  
Texas Instrument

# What comes next ?

- Almost all the important processes and devices in micro-scale already existed 10 years ago, e.g. DRIE, bonding, comb-drive, SDA, etc.



- **Technological sophistication,**
- **Application diversity** increase
- **Performance** improvement.
- **Commercial products** have flourished.



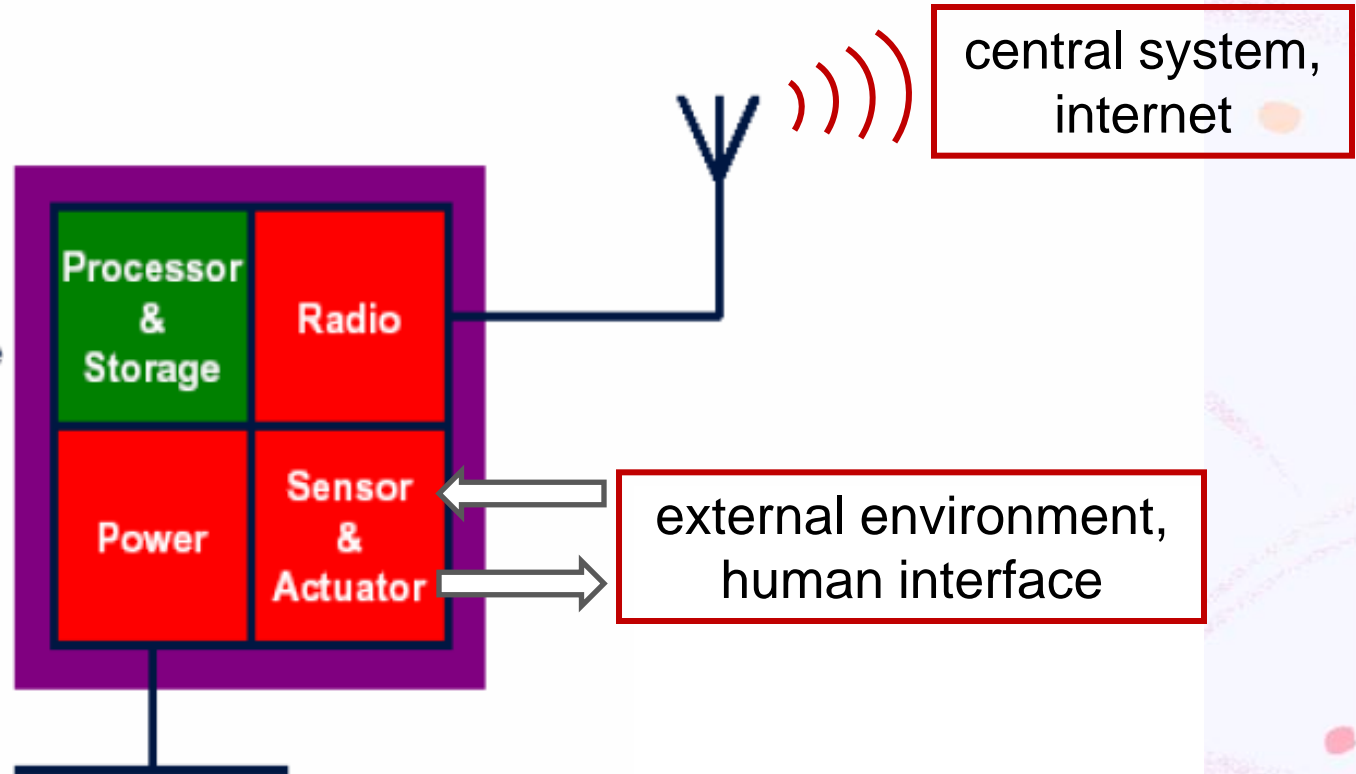
- In order to widen the application fields, heterogeneous integration of various functionalities becomes important. (More than Moore approach)



Intelligent systems incorporate 'More Moore' and 'More than Moore'

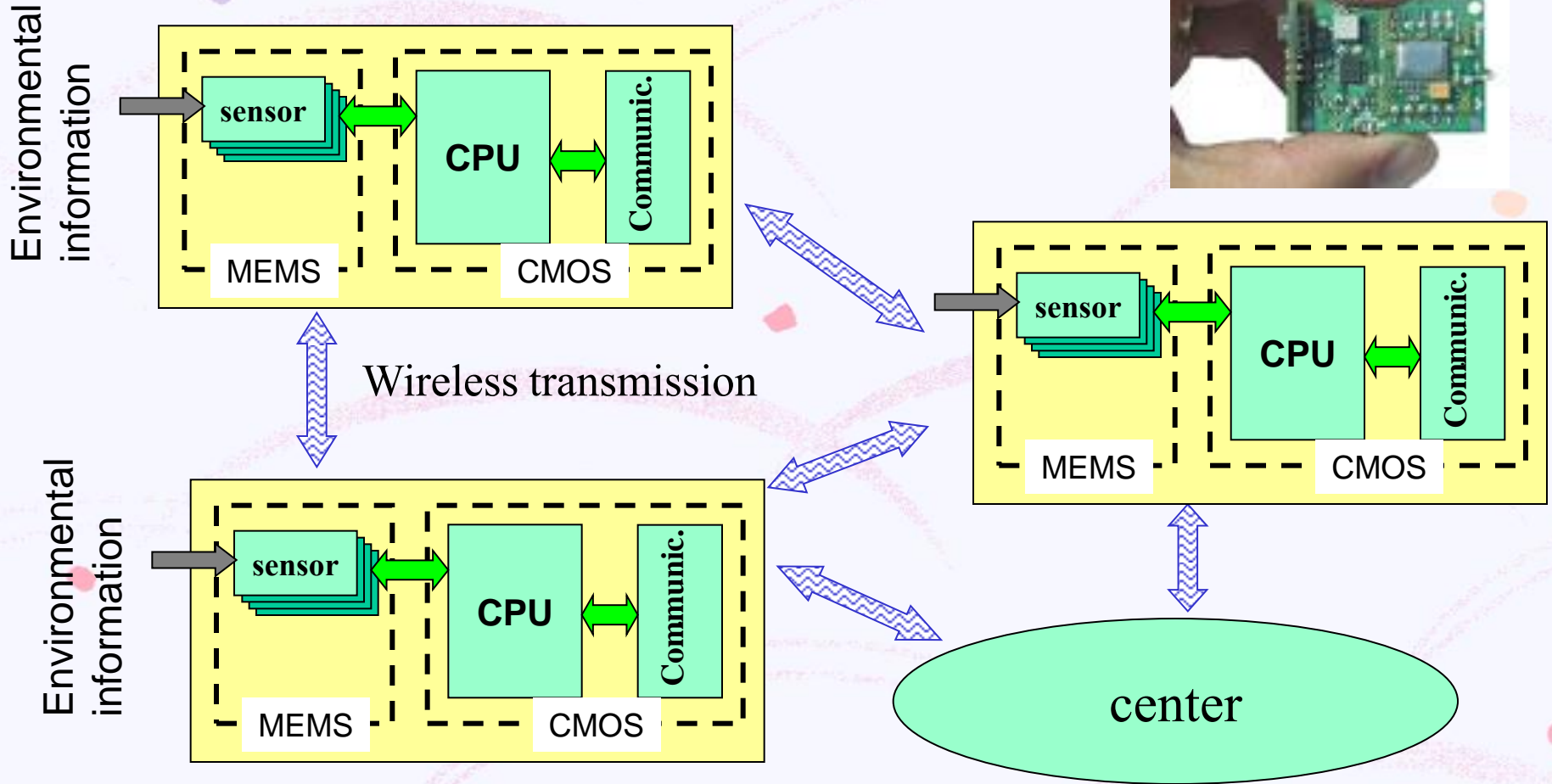
- More and beyond Moore
- More than Moore
- Hetero Integration

MEMS technology



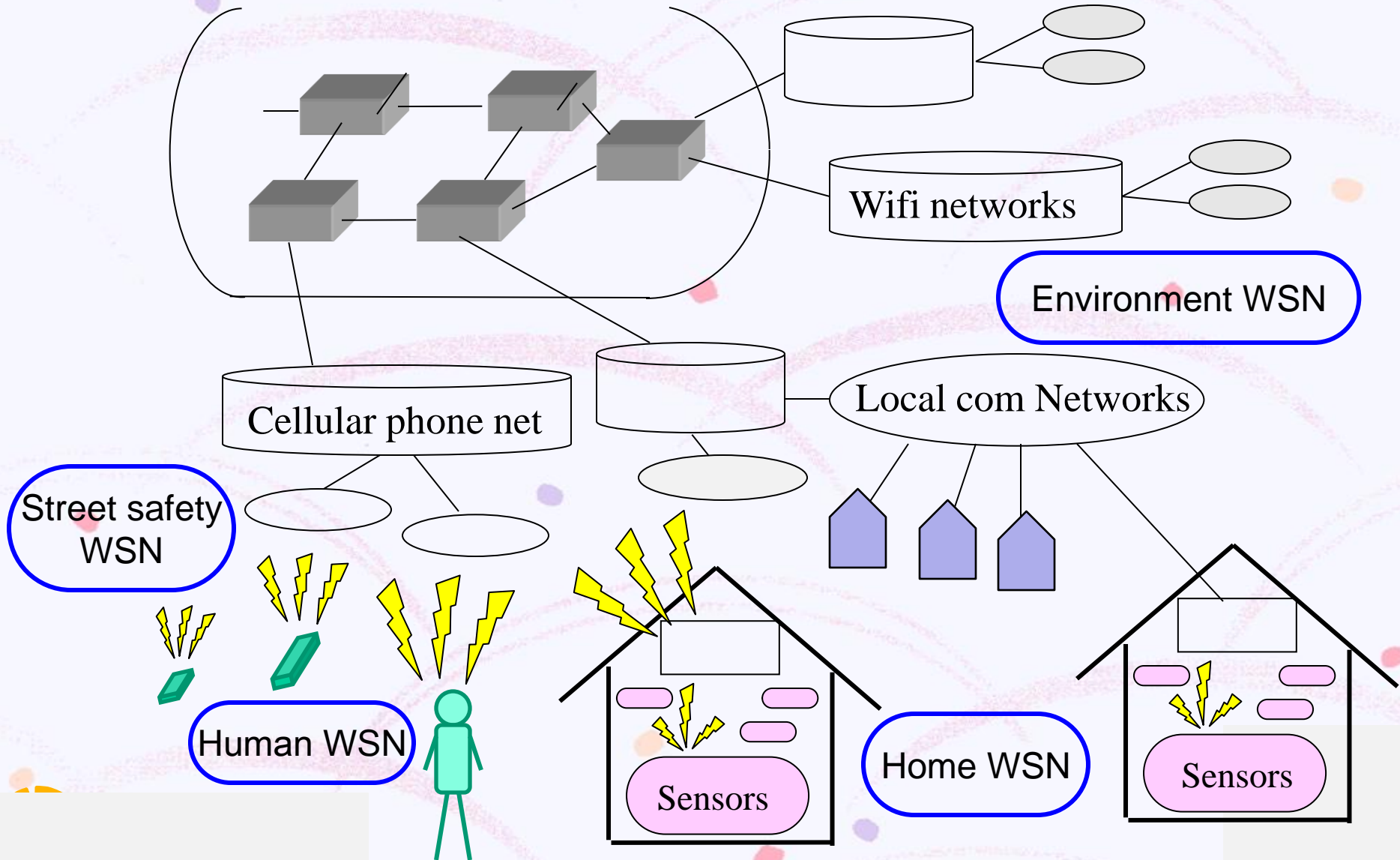
More than Moore, 2005/09/16

# Micro wireless sensor network





# MEMS wireless sensor net (WSN) in communication hierarchy



# Content

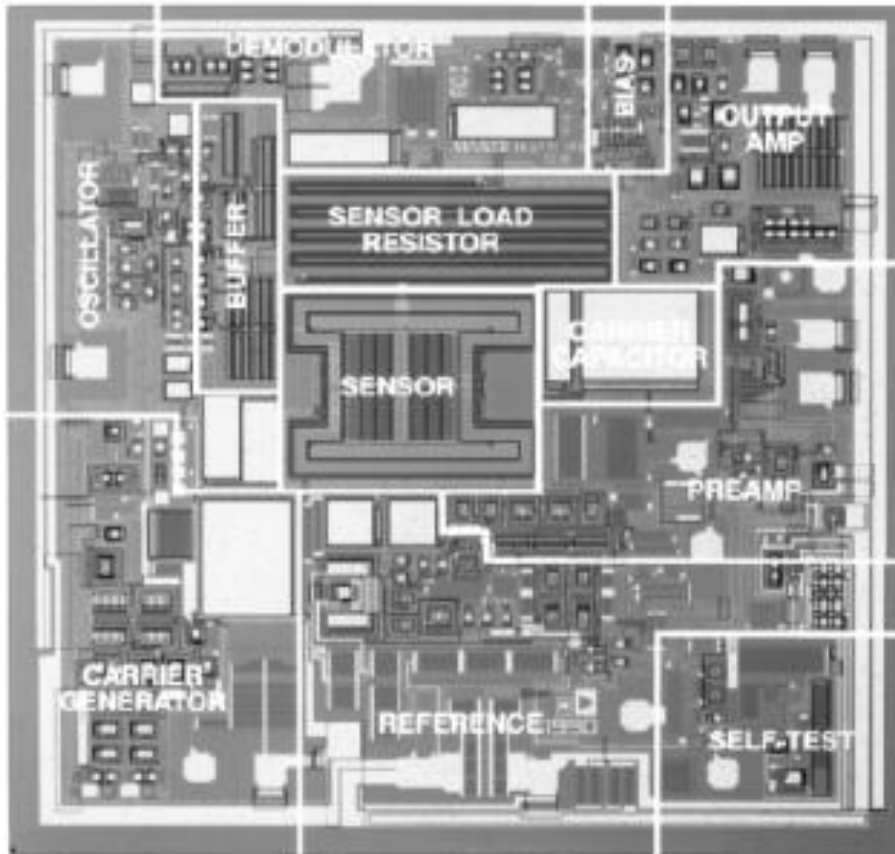
- MEMS trend toward MEMS-CMOS integration
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# MEMS-CMOS integration methods

- **Hybrid integration**, especially stack integration using TSV
- Monolithic integration by customized **fully mixed process**
- Monolithic integration by **MEMS processing first** followed by CMOS process
- Monolithic integration by **CMOS processing first** followed by MEMS process

# CMOS-MEMS by surface micromachining

## ADXL-50 Chip Diagram



Analog Devices' ADXL-50, the industry's first surface micromachined accelerometer, includes signal conditioning on chip.

- Fully mixed fabrication process.
- Poly-Si structure + SiO<sub>2</sub> sacrificial layer.
- Protection of circuits while releasing process is important.



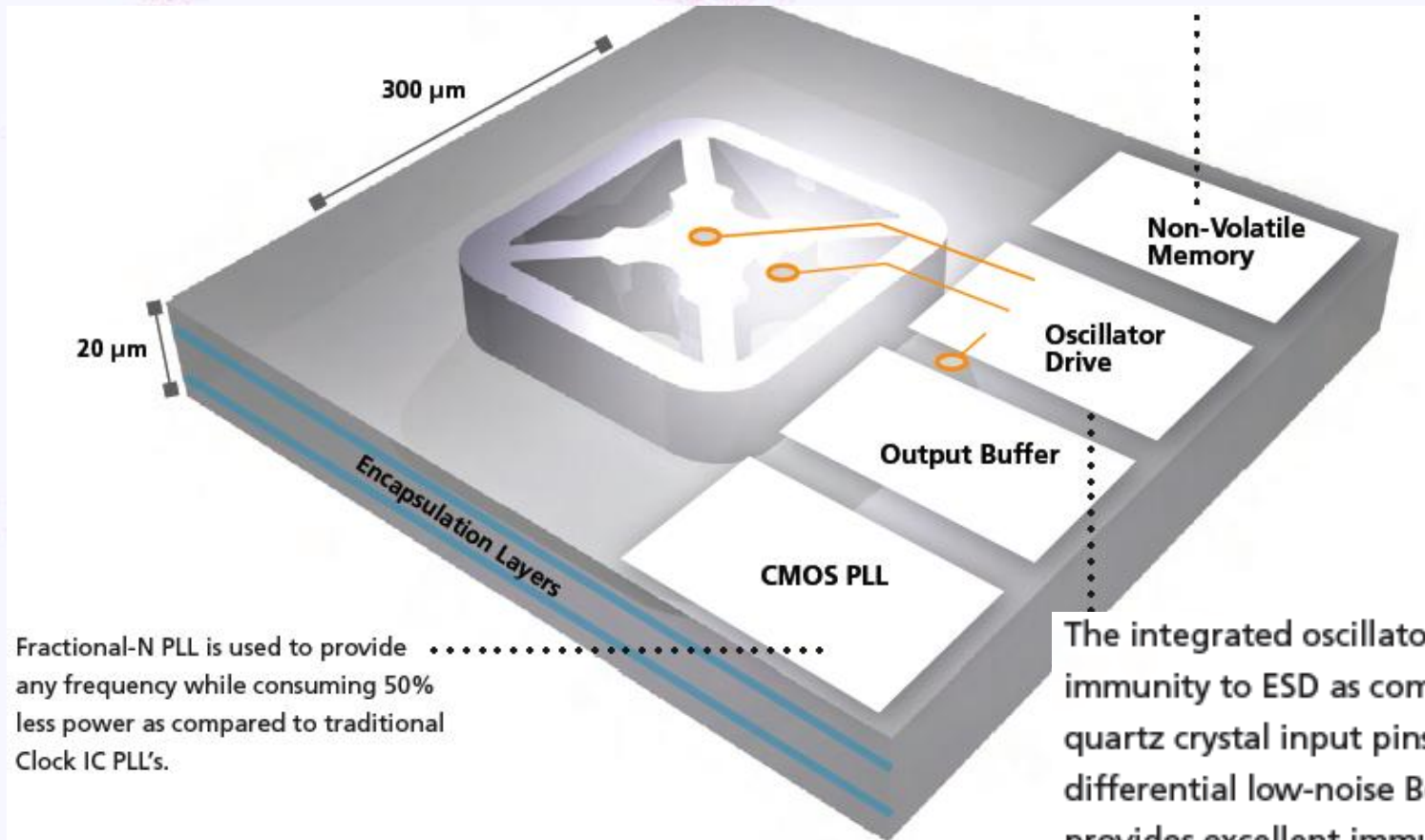
# MEMS-CMOS integration methods

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- **Monolithic integration by MEMS processing first followed by CMOS process**
- Monolithic integration by CMOS processing first followed by MEMS process

# SiTime MEMS resonator

## MEMS-first approach for CMOS circuit integration

Non-Volatile memory enables rapid configuration of the SiT8002 family to instantly match the form, fit, and function of 100's of fixed frequency oscillators. In addition, the memory never wears out and requires no additional CMOS mask layers, keeping costs low.

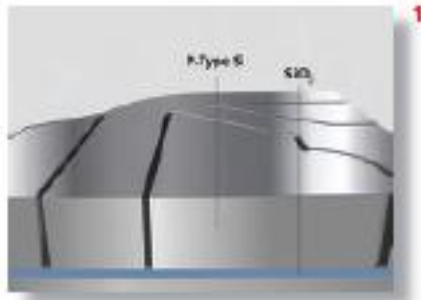


Fractional-N PLL is used to provide ..... any frequency while consuming 50% less power as compared to traditional Clock IC PLL's.

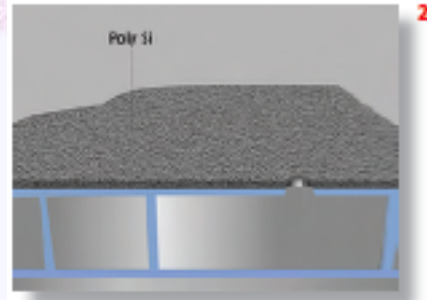
The integrated oscillator provides better immunity to ESD as compared to many quartz crystal input pins. In addition, the differential low-noise Boser Oscillator provides excellent immunity to electrical interference as compared to single-ended quartz devices.

# SiTime MEMS resonator

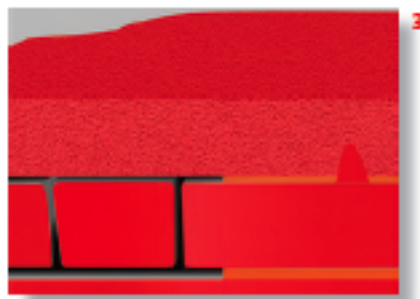
## M E M S-first approach for CMOS circuit integration



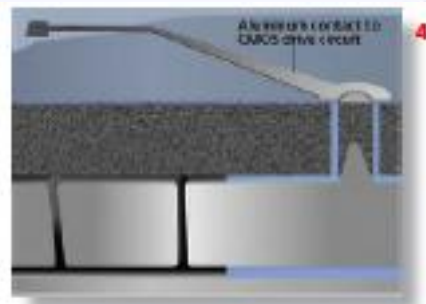
1  
DRIE of SOI defining resonator (0.4um wide, 10um deep). Trenches filled by SiO<sub>2</sub>



2  
Thin epi-poly growth. Contacts and etch holes formation.

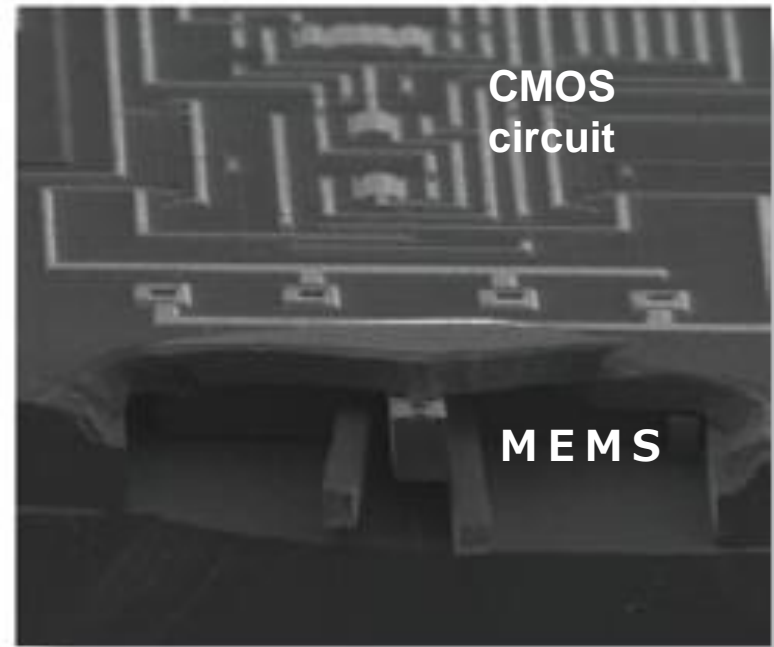


3  
After sacrificial etching of SiO<sub>2</sub>, thick epi-poly growth.



4  
Surface polishing and cleaning for next CMOS process. Contact isolation by DRIE

Single crystal Si encapsulation layer allows CMOS integration



**SiTime™**

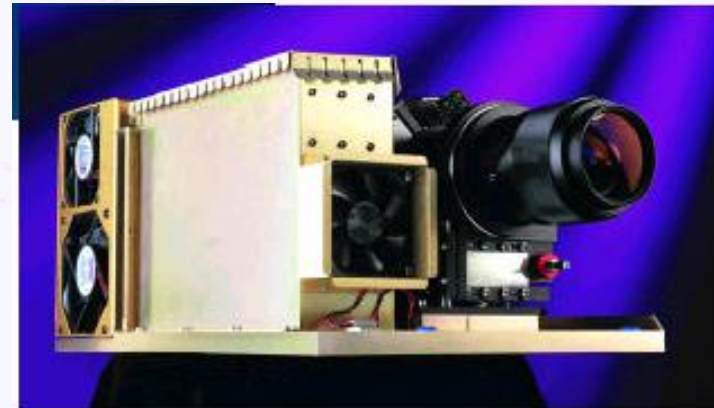
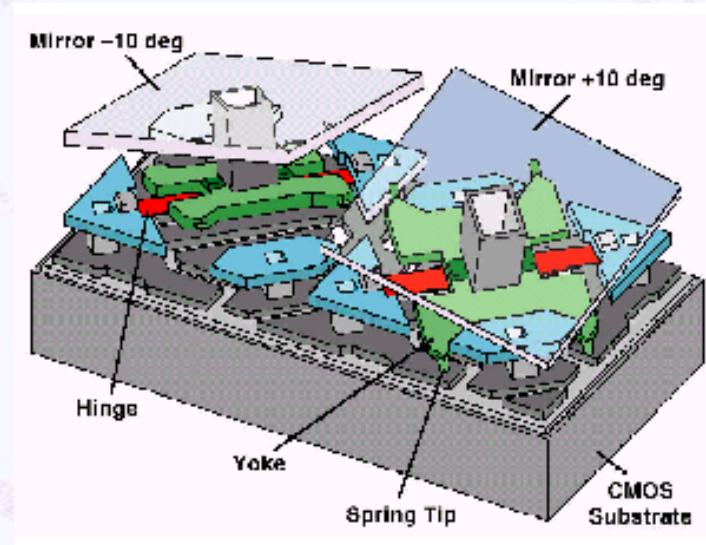
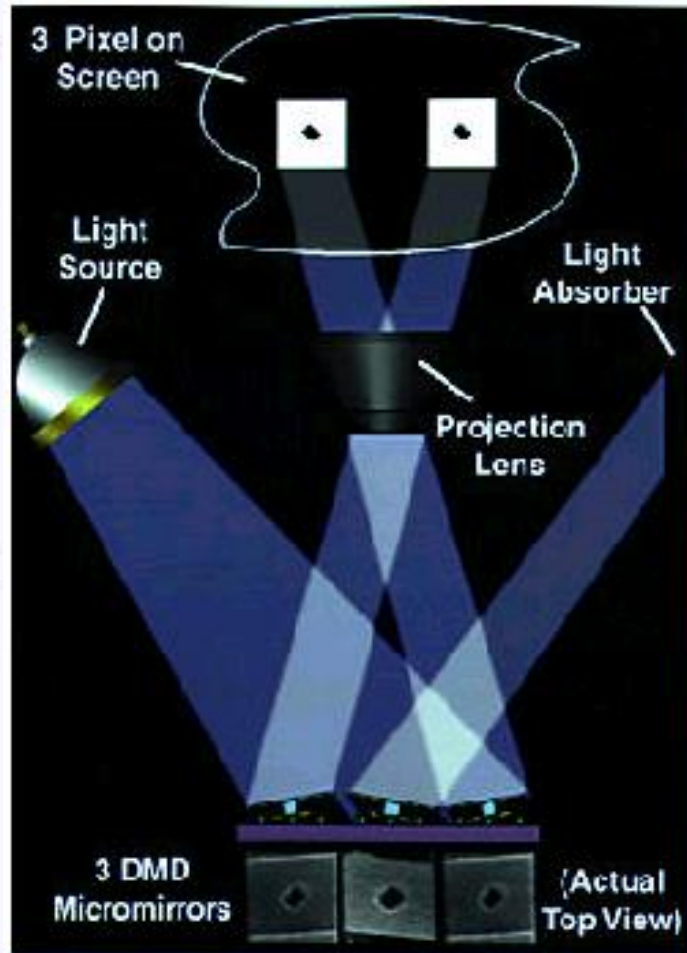
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- Monolithic integration by CMOS processing first followed by MEMS process



# DIGITAL MIRROR DISPLAY (1)

P.F. Van Kessel et al., T.I., Proc. IEEE, Vol. 86, p 1687, 1998



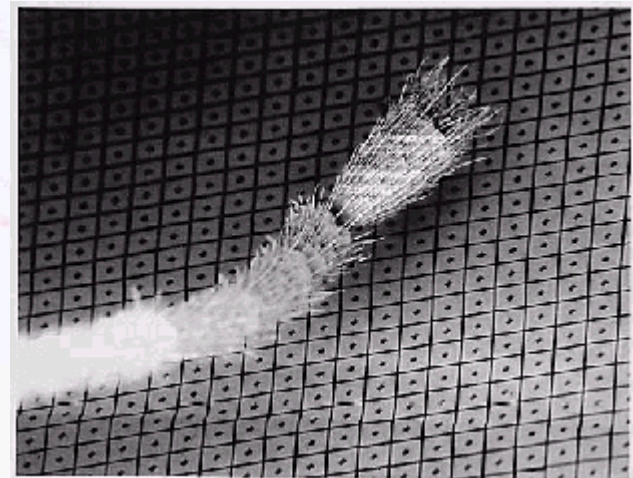
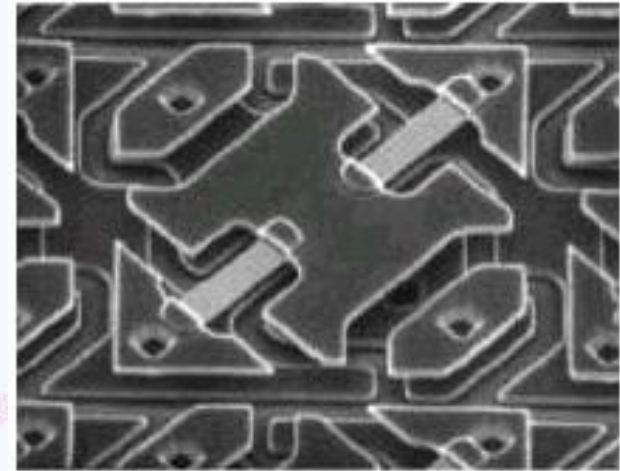
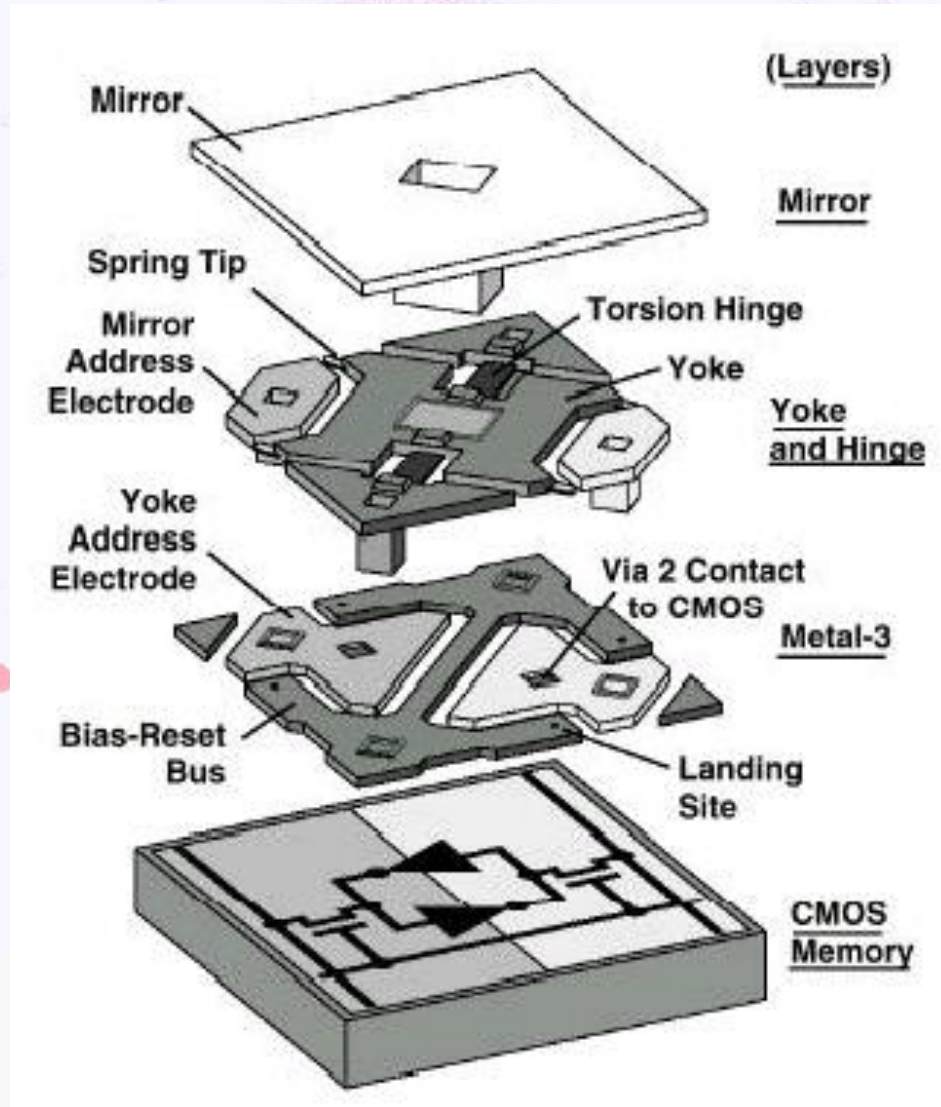
# DIGITAL MIRROR DISPLAY (video)

P.F. Van Kessel et al., T.I., Proc. IEEE, Vol. 86, p 1687, 1998



# DIGITAL MIRROR DISPLAY (2)

P.F. Van Kessel et al., T.I., Proc. IEEE, Vol. 86, p 1687, 1998





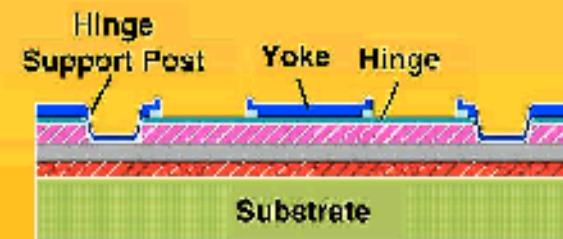
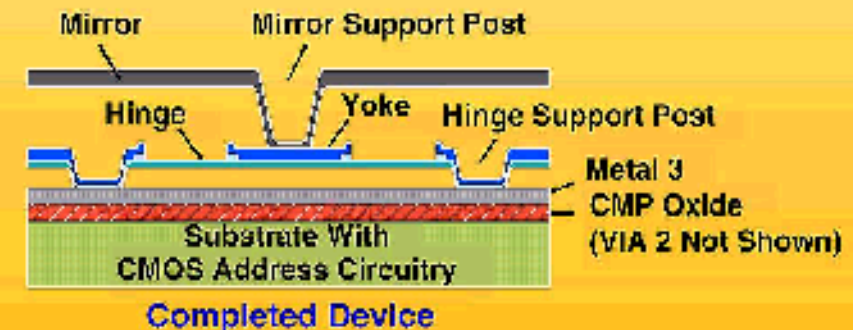
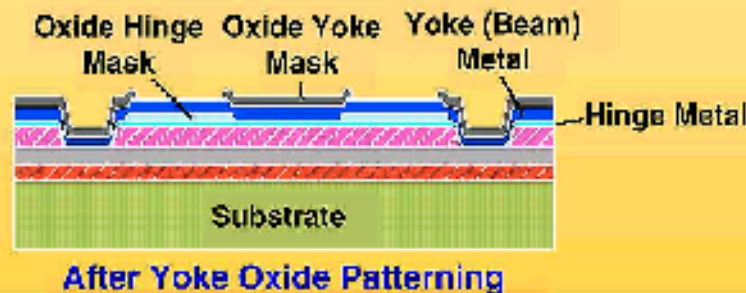
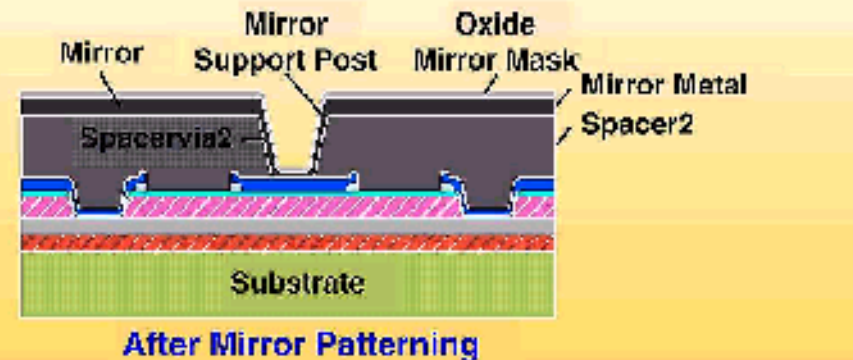
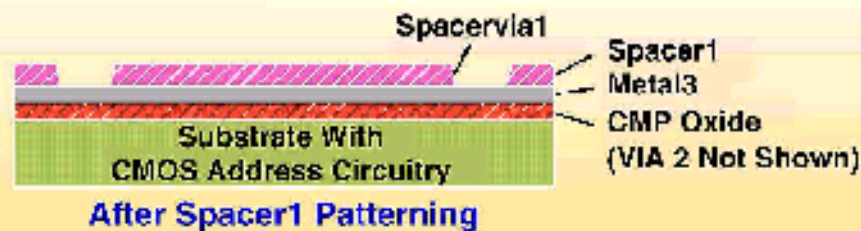
# DIGITAL MIRROR DISPLAY (3)

P.F. Van Kessel et al., T.I., Proc. IEEE, Vol. 86, p 1687, 1998

Al mirror ---- CMOS Process compatible

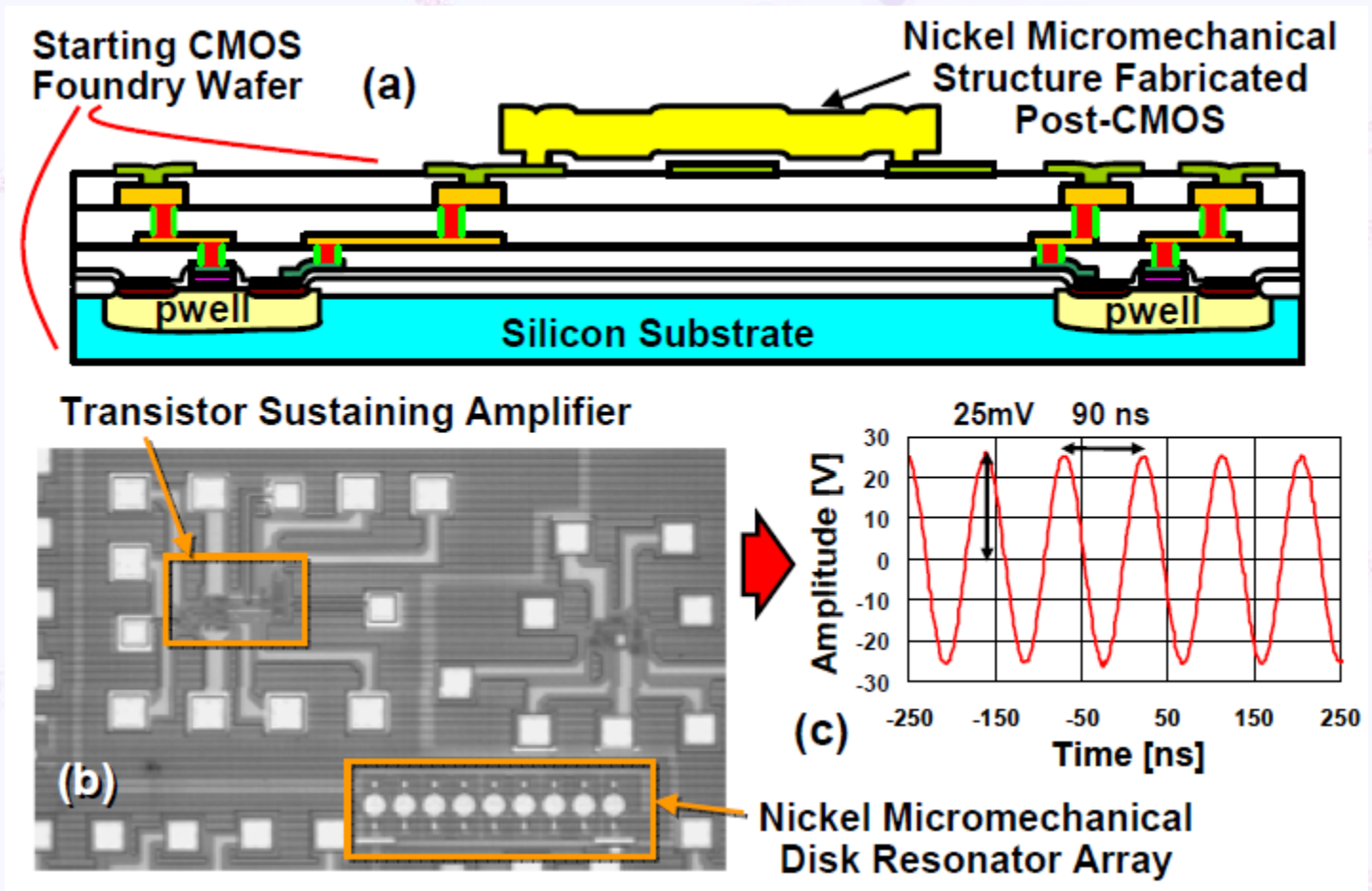
Photoresist sacrificial layer --- removed by plasma etching

DMD on CMOS SRAM by 6 mask process





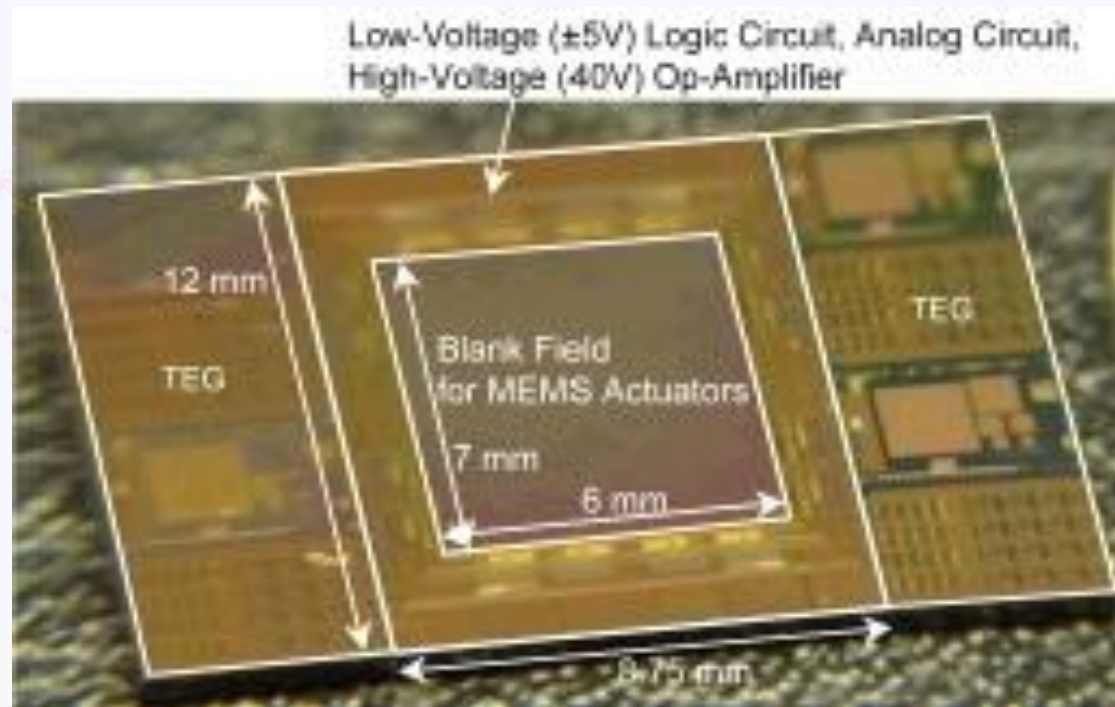
# Post-CMOS metal structure



- (a) Cross-section of the nickel MEMS-transistor integration process.  
 (b) Die photo of a fully monolithic micromechanical resonator oscillator using this process. (c) Oscilloscope waveform.

# Post-CMOS MEMS by Deep-RIE

Some space (7 mm x 6 mm) in 40V high-voltage chip is left for post processing of MEMS. MEMS devices are made in 8 $\mu$ m-thick active layer of SOI substrate by deep RIE. Handling layer of 625 $\mu$ m in thickness can also be structured by RIE. Each of four CMOS segments includes a 16-bit demultiplexer, a 12-bit DA converter, four operational amplifier with sample & holder.



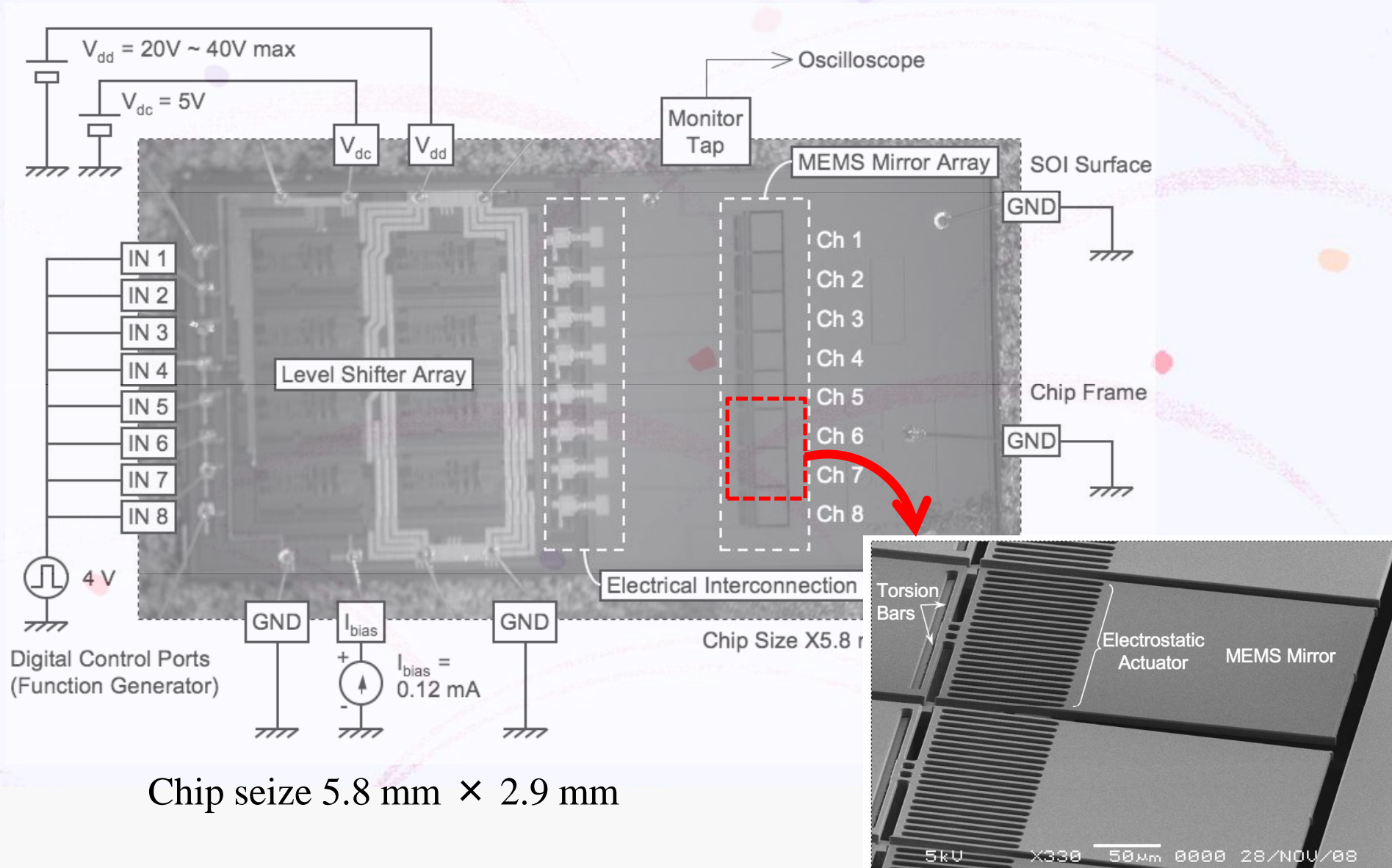
Source: Toshiyoshi Lab. IIS, University of Tokyo

# A MEMS Digital Mirror Array Integrated with High-voltage Level-shifter

*S. Maruyama, K. Takahashi, H. Fujita and H. Toshiyoshi*

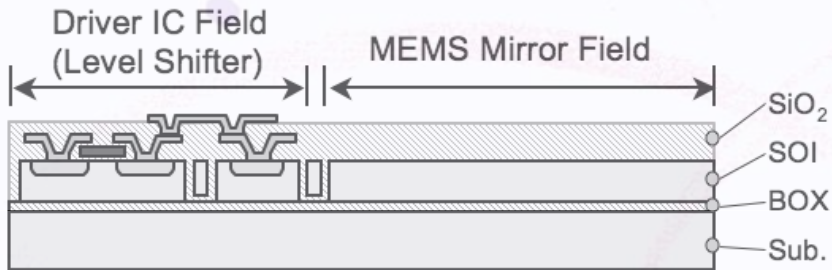
● Institute of Industrial Science, The University of Tokyo, Tokyo, Japan

# CMOS-MEMS mirror array

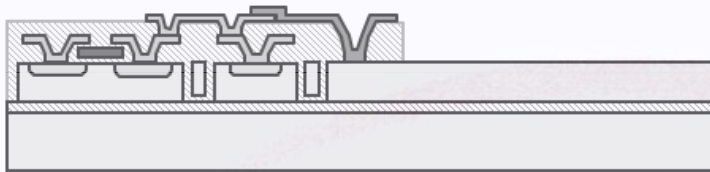




# Post-CMOS MEMS fabrication

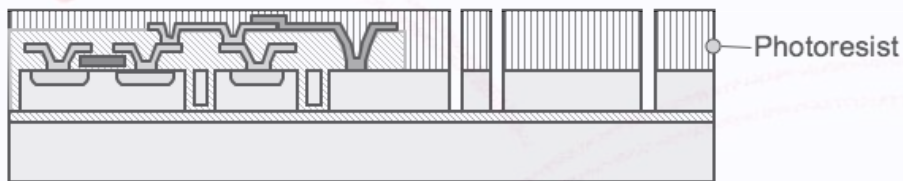


(1) As delivered pre-fabricated CMOS

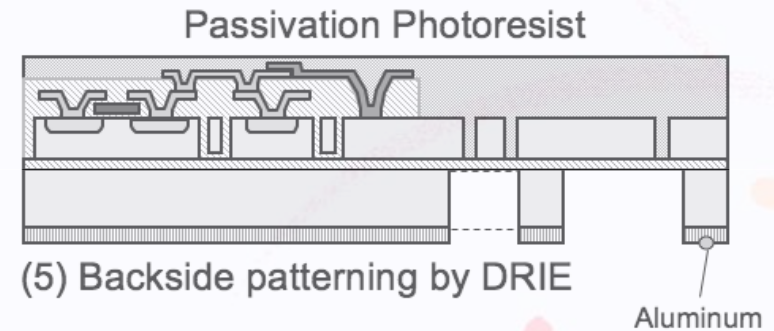


(2) Removal of field oxide

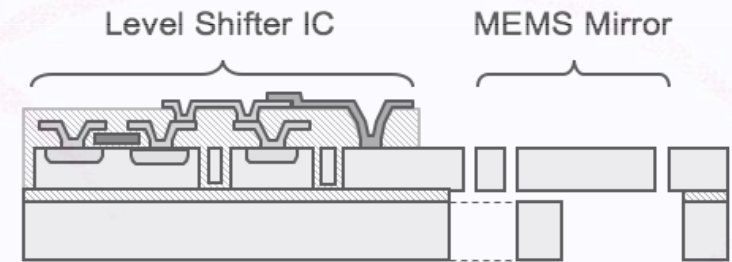
(3) CMOS-MEMS interconnection



(4) SOI patterning by DRIE

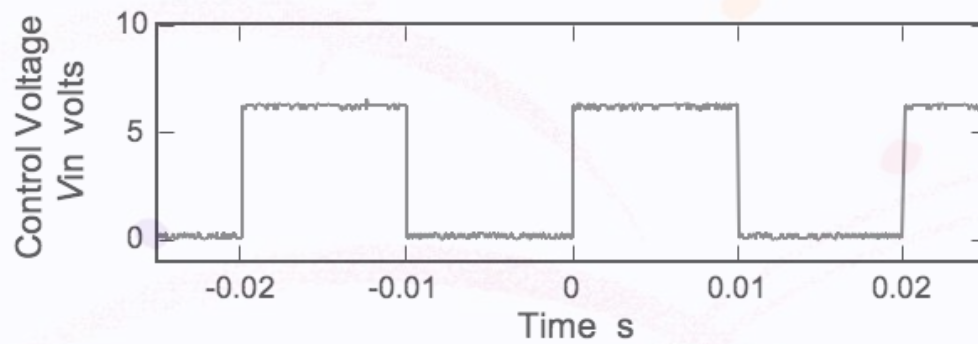


(5) Backside patterning by DRIE



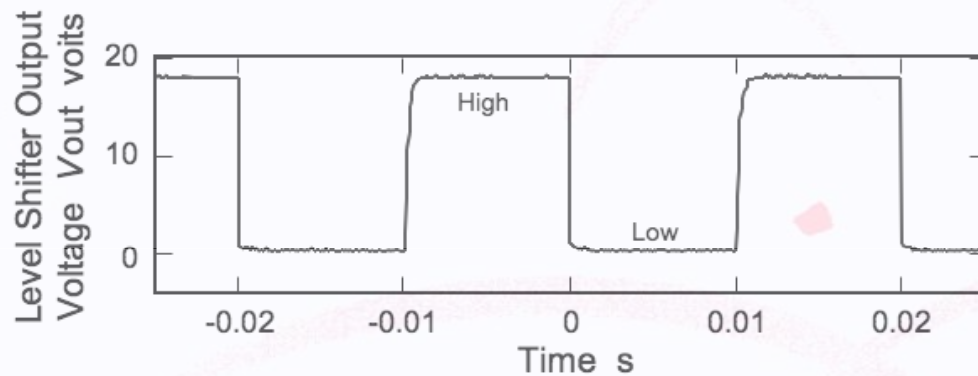
(6) Sacrificial BOX release in HF

## Operation result



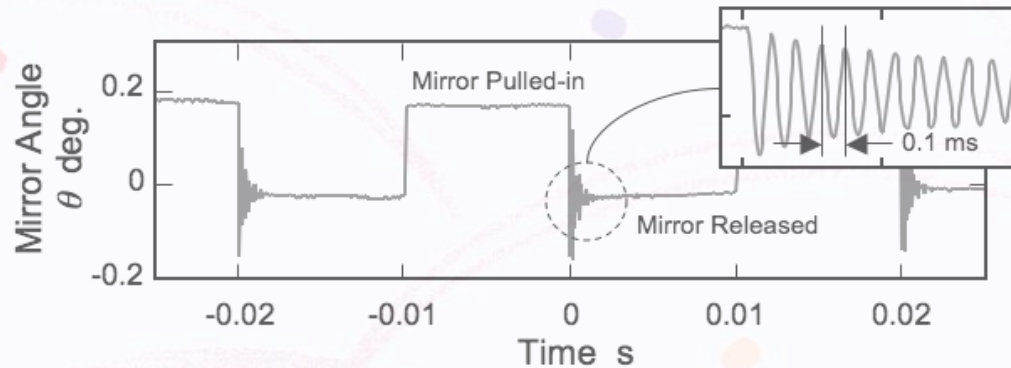
(a)

(a) input voltage to the level shifter



(b)

(b) output voltage of the level shifter



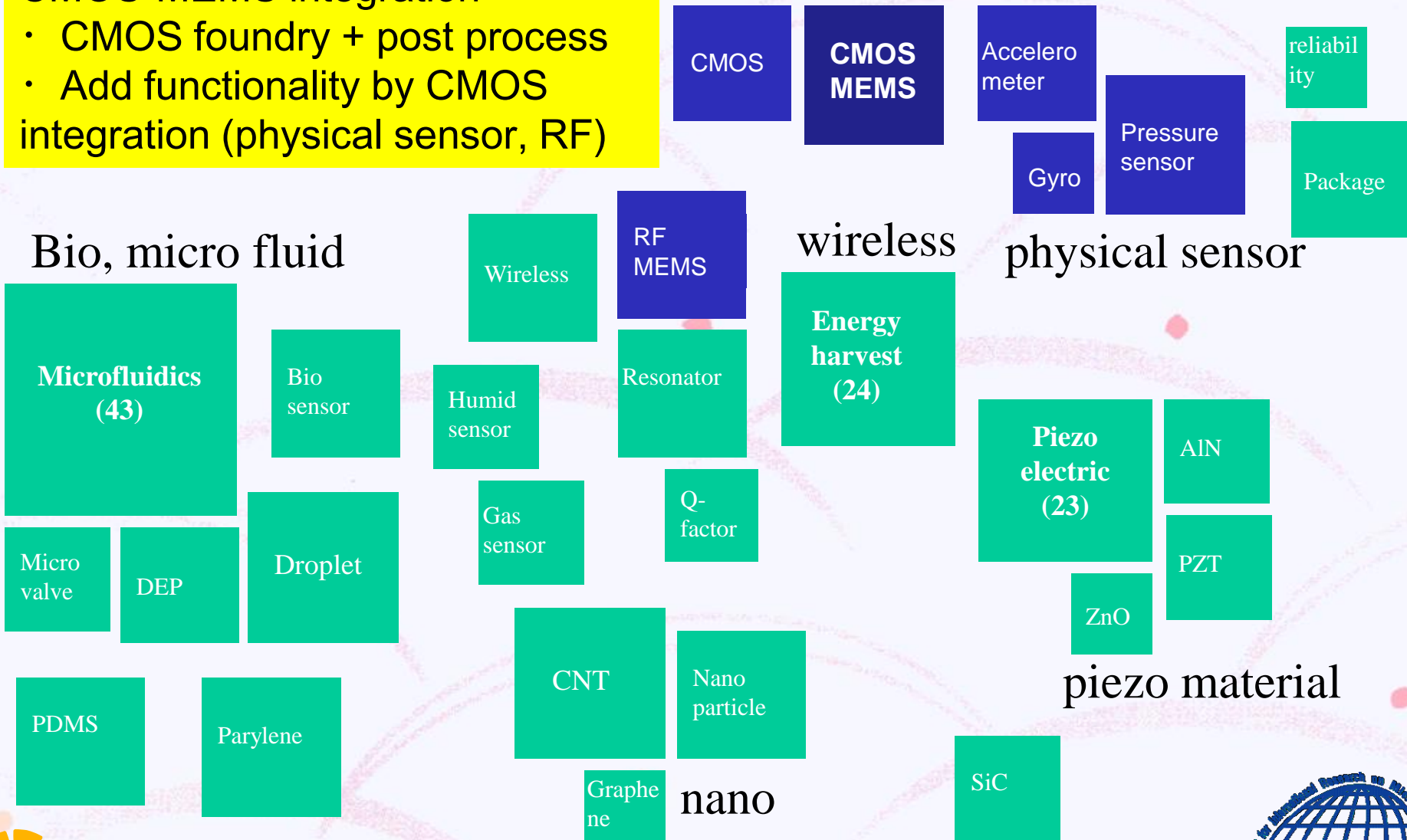
(c)

(c) mirror angle.

# Keyword statistics at Transducers 2011

**CMOS-MEMS integration**

- CMOS foundry + post process
- Add functionality by CMOS integration (physical sensor, RF)

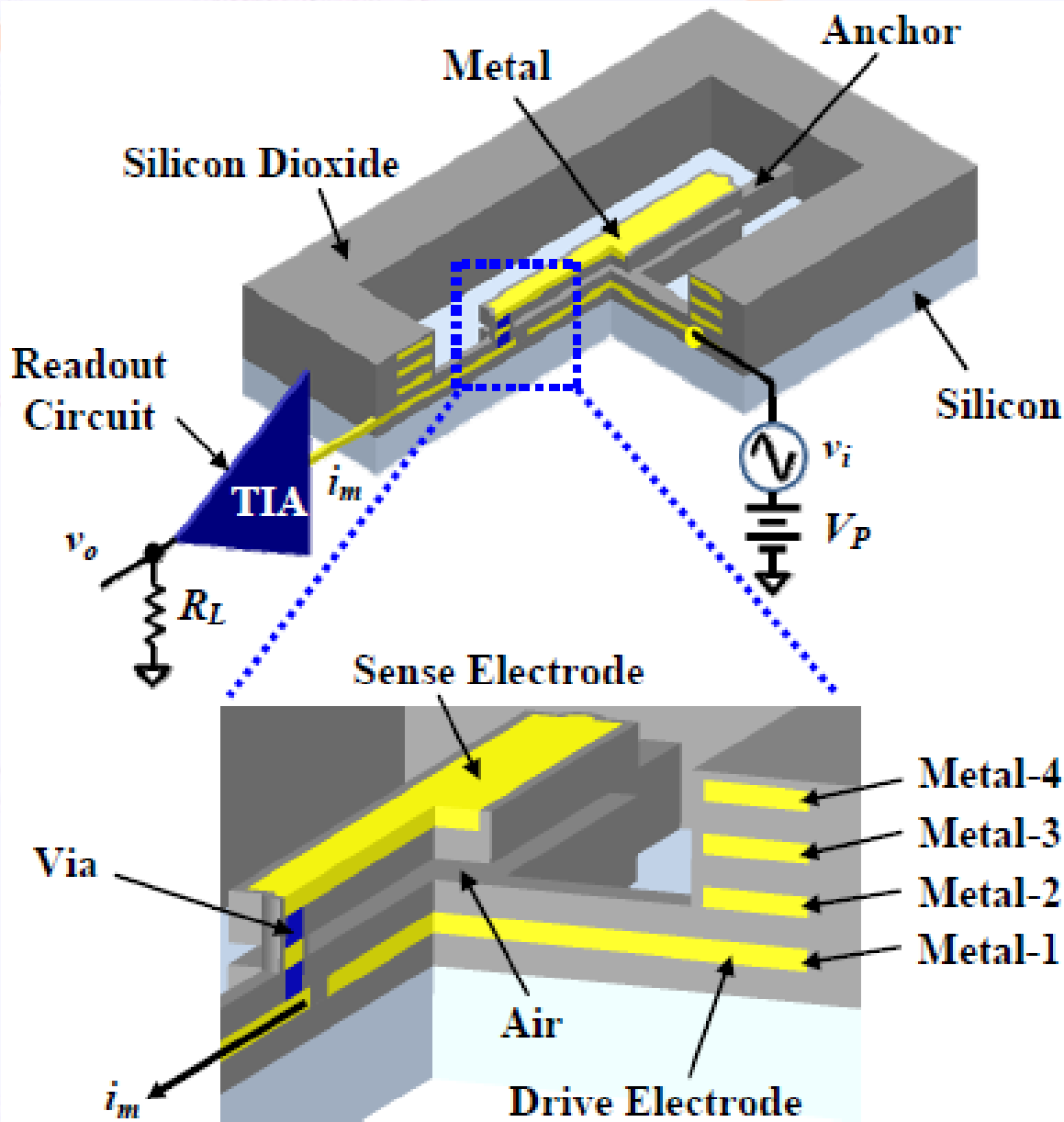


# High-q, Large-Stopband-Rejection Integrated CMOS-MEMS Oxide Resonators with Embedded Metal Electrodes

*Yu-Chia Liu<sup>1</sup>, Ming-Han Tsai<sup>1</sup>, Wen-Chien Chen<sup>2</sup>, Sheng-Shian Li<sup>1,2</sup> and  
Weileun Fang<sup>1,2</sup>*

<sup>1</sup> Inst. of NanoEngineering and MicroSystems and  
<sup>2</sup> Dept. of Power Mechanical Engineering  
National Tsing Hua University, Hsinchu, Taiwan

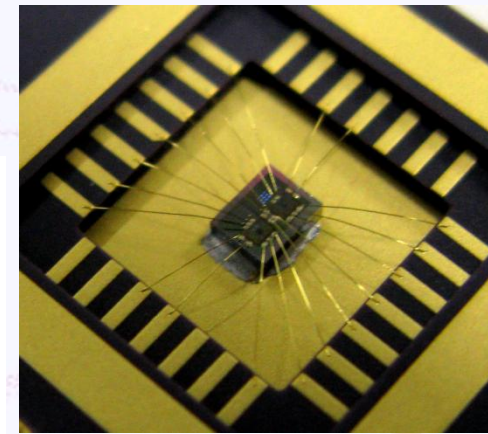




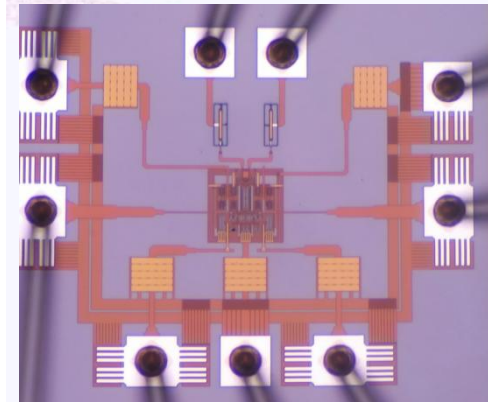
Perspective-view schematic of an electrode-embedded CMOS-MEM oxide resonator, including zoom-in of quarter cross-section view with signal transmission in a one-port test configuration.

*Table 1: Design Parameters of the Capacitively-Transduced CMOS-MEMS Oxide Resonator.*

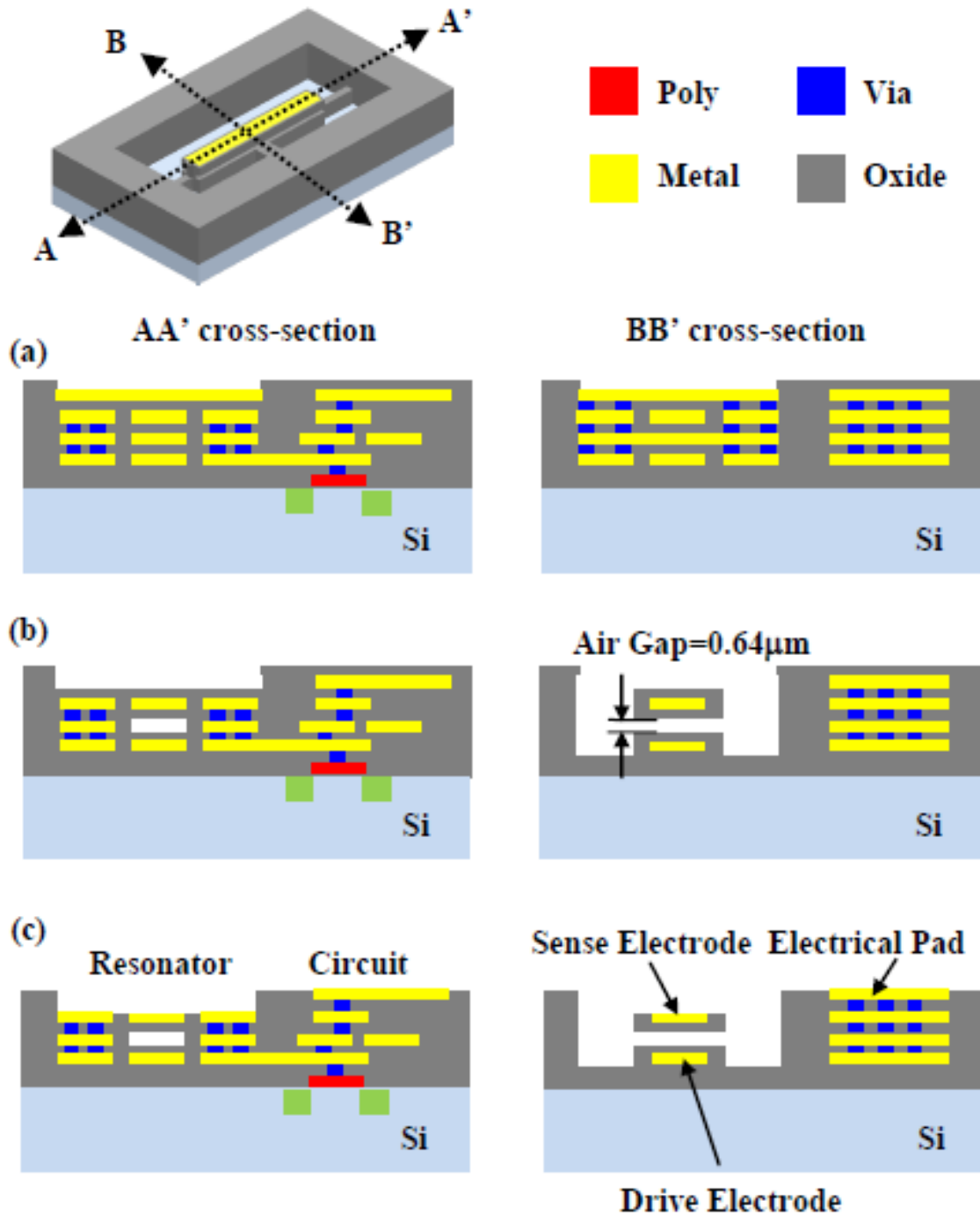
Design Parameter	Value	Unit
Beam Length, $L_r$	55	$\mu\text{m}$
Beam Width, $W_r$	4	$\mu\text{m}$
Air Gap, $d_o$	0.64	$\mu\text{m}$
Oxide Thickness, $h_{ox}$	1	$\mu\text{m}$
Structure Thickness, $H_r$	1.64	$\mu\text{m}$
Effective Mass, $m_r$	0.0388	nkg
Spring Constant, $k_r$	102	N/m
Resonance Frequency (Calculation)	2.58	MHz
Resonance Frequency (Simulation)	2.54	MHz



*CMOS-MEMS chip in ceramic housing.*



*Die photo of monolithic CMOS-MEMS integration.*



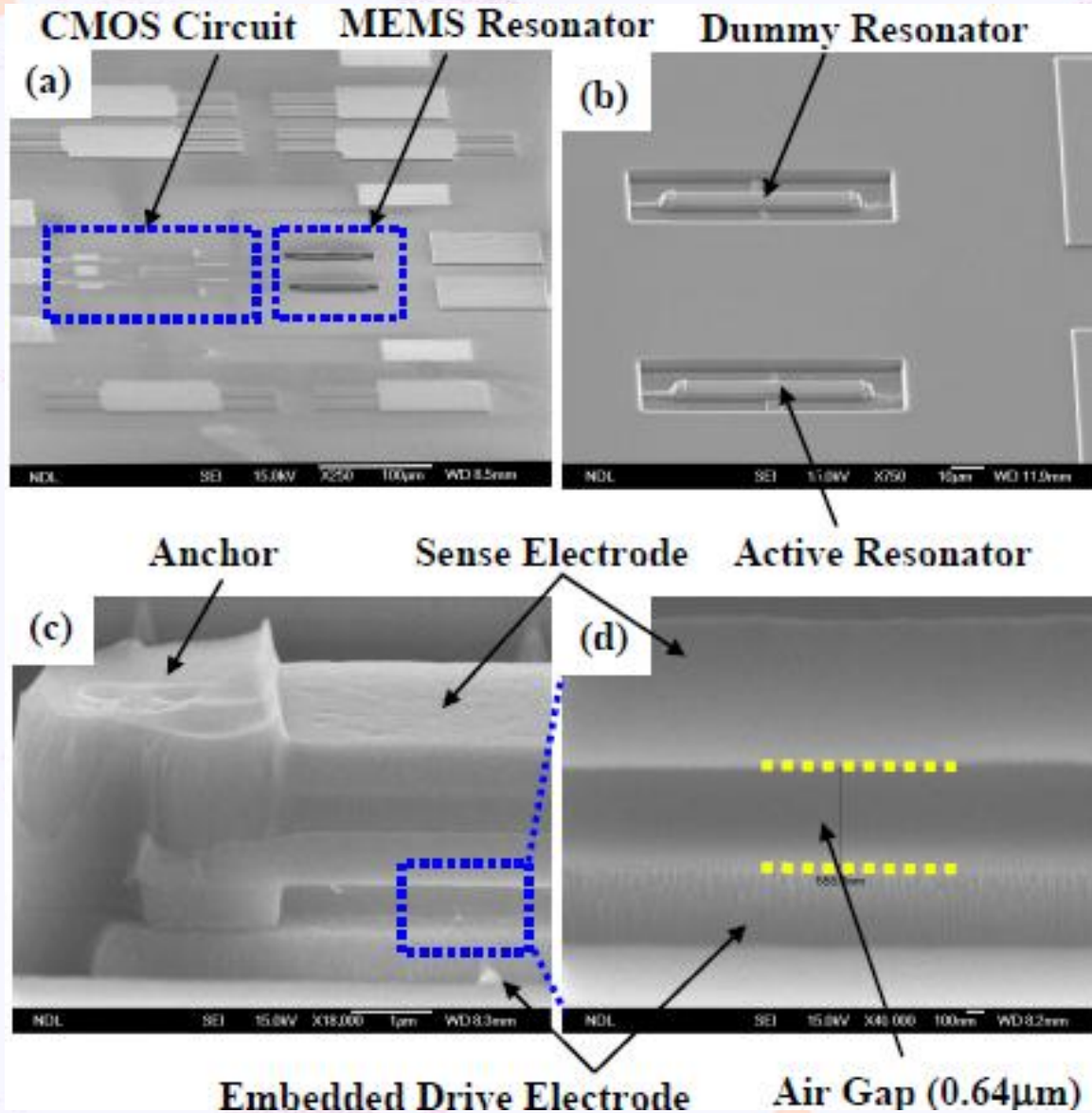
## Fabrication sequence

(a) a chip manufactured by standard TSMC 0.35  $\mu\text{m}$  2P4M process,

(b) metal wet etching to form resonator structure and transducer's gap, and

(c) RIE dry etch to open the electrode pads.

Transducers' 11, Beijing, China,  
June 5-9, 2011, p. 934



## SEM views

(a) CMOS-MEMS integration

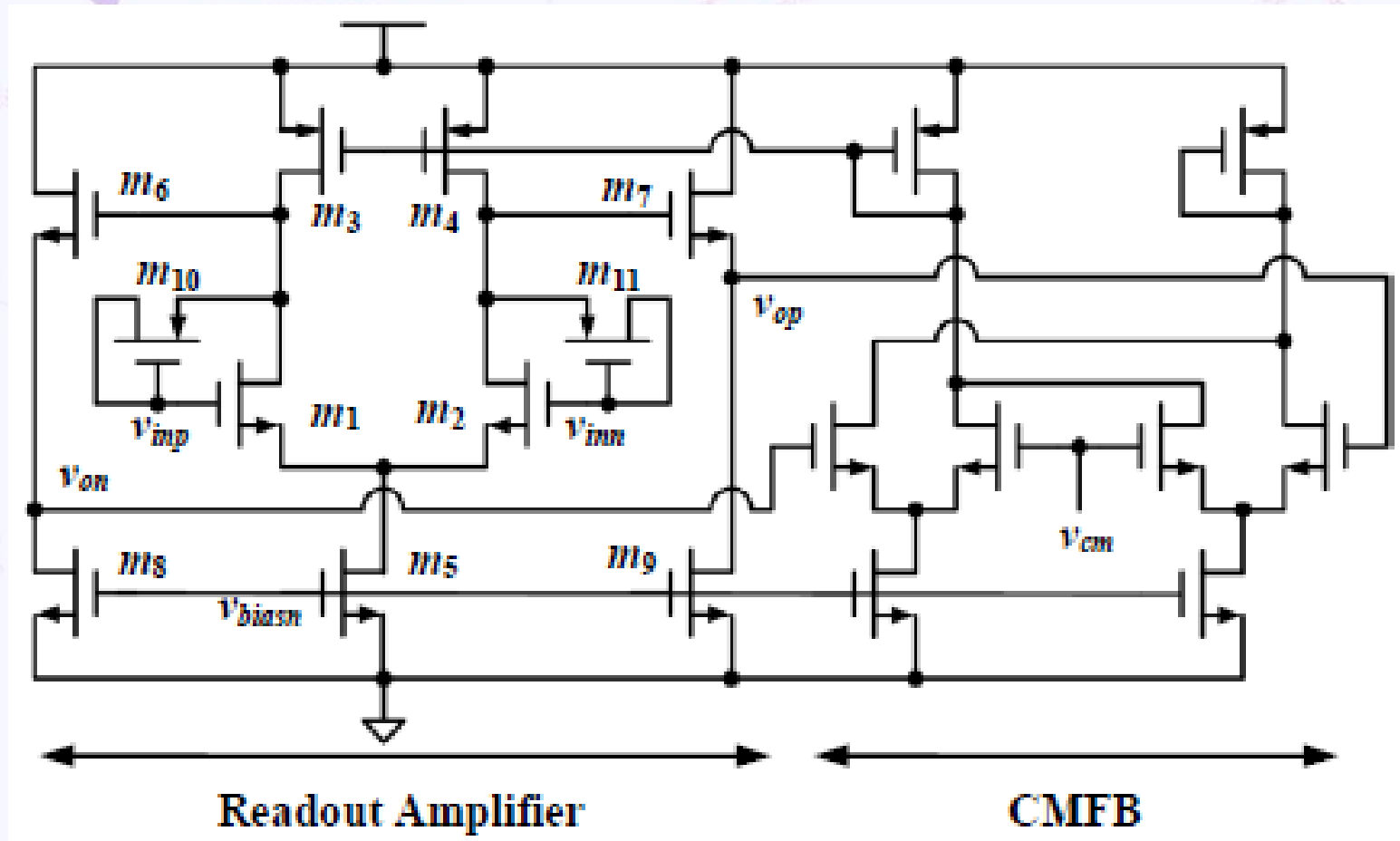
(b) dummy device to suppress parasitic feed-through

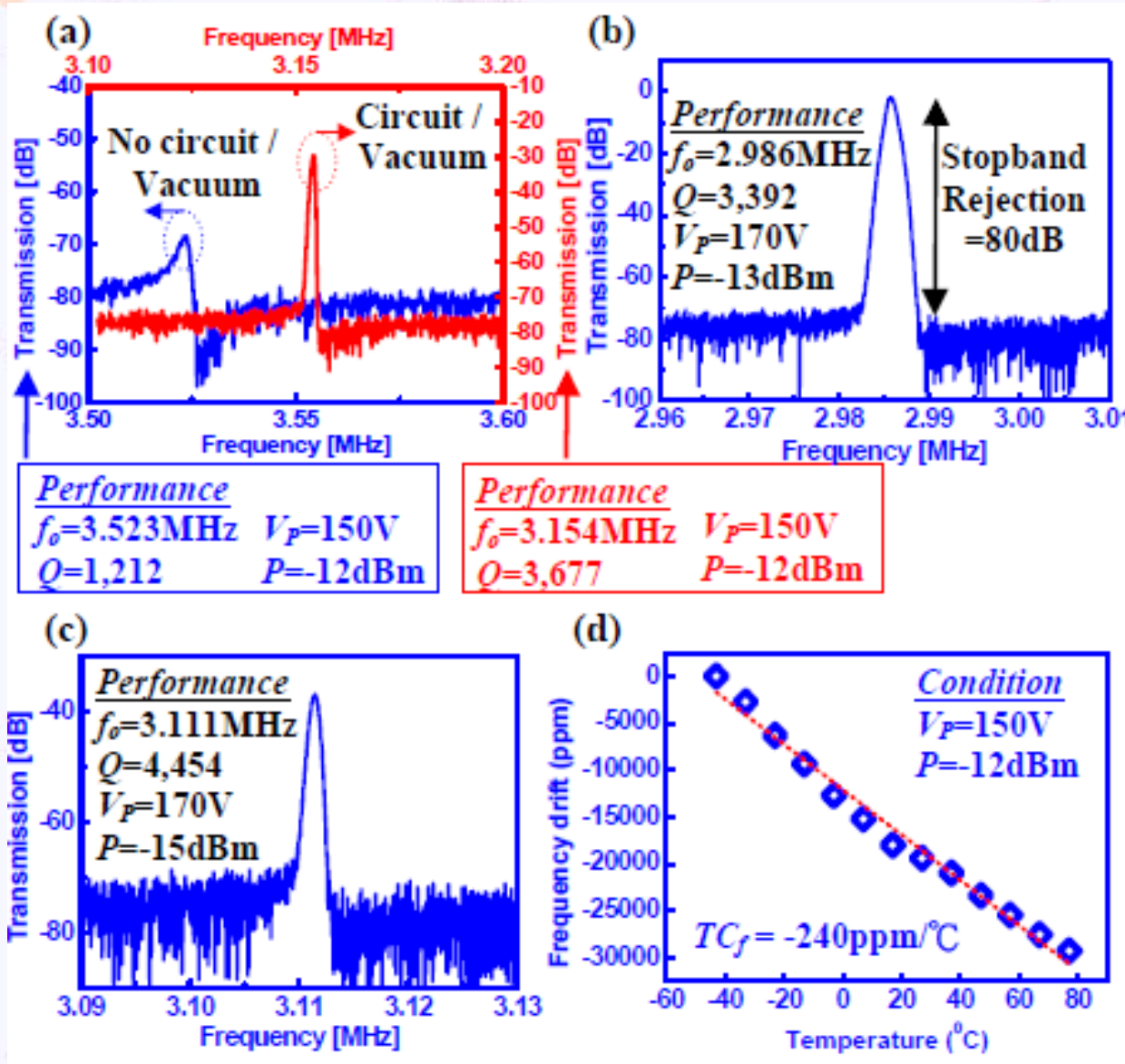
(c) zoom-in of the out-of-plane resonator

(d) zoom-in of air gap



# Schematic diagrams of a fully-differential readout amplifier.





## Measurement results

(a) with/without circuit tested in vacuum,

(b) frequency response with the highest stopband rejection,

(c) frequency response with the highest Q value,

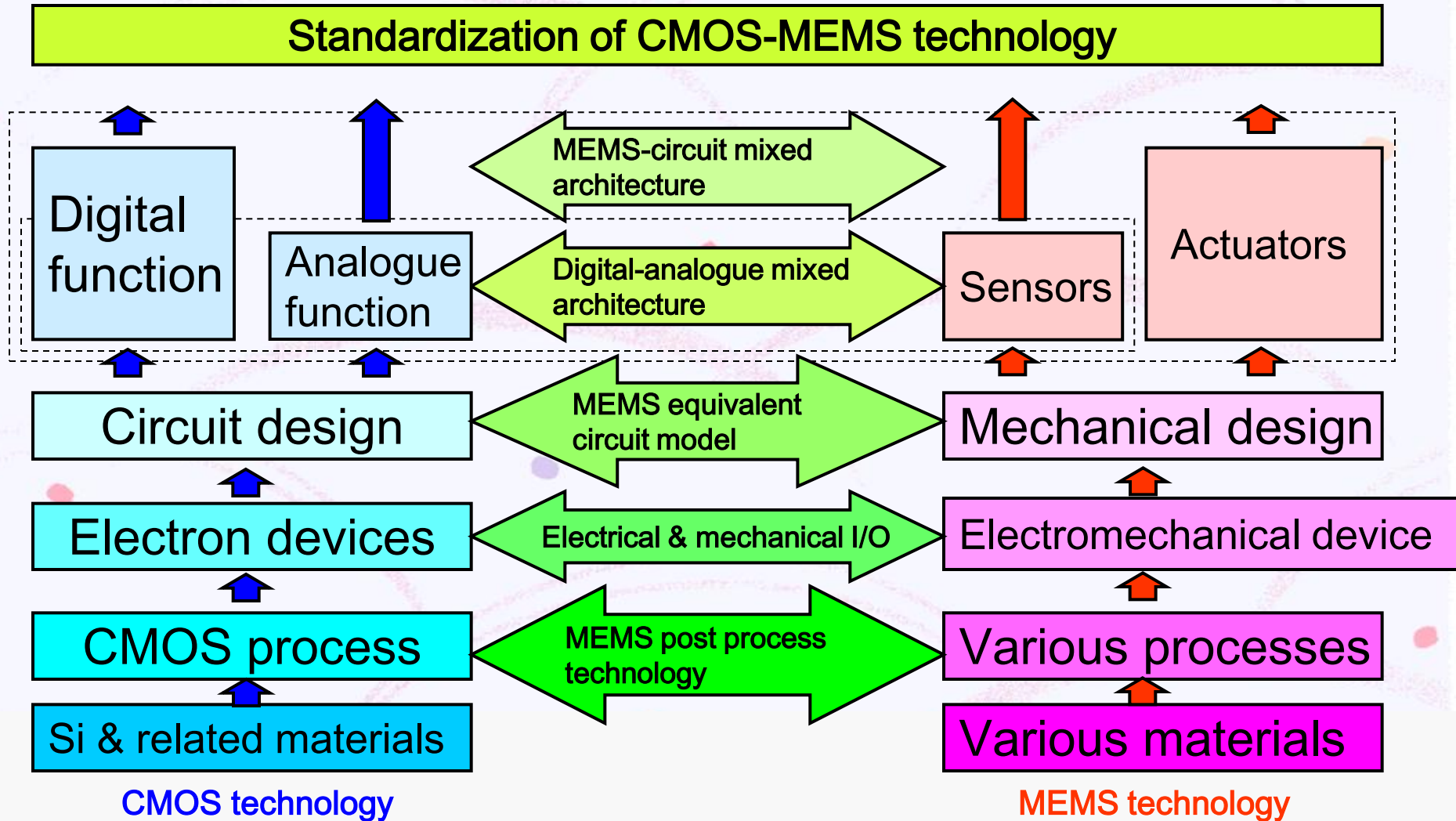
(d) measured fractional frequency change versus temperature.

*Table 2: CMOS-MEMS-Based Resonator Summary.*

	<b>This work</b>	Ref [3]	Ref [5]	Ref [4]
Type	<b>CC-Beam</b>	Beam	SFR	FF-Beam
Materials	<b>Metal + Oxide</b>	Metal + Oxide	Metal + Oxide	Metal + Oxide
$f_o$ (MHz)	<b>3.11</b>	6.33	6.18	14.5
$Q$	<b>~3,300-4,400</b>	~100*	~1,000	~1,500
$SB$ rej. (dB)	<b>~40-80</b>	~4	~14	~10

\*Measured in atmospheric pressure.

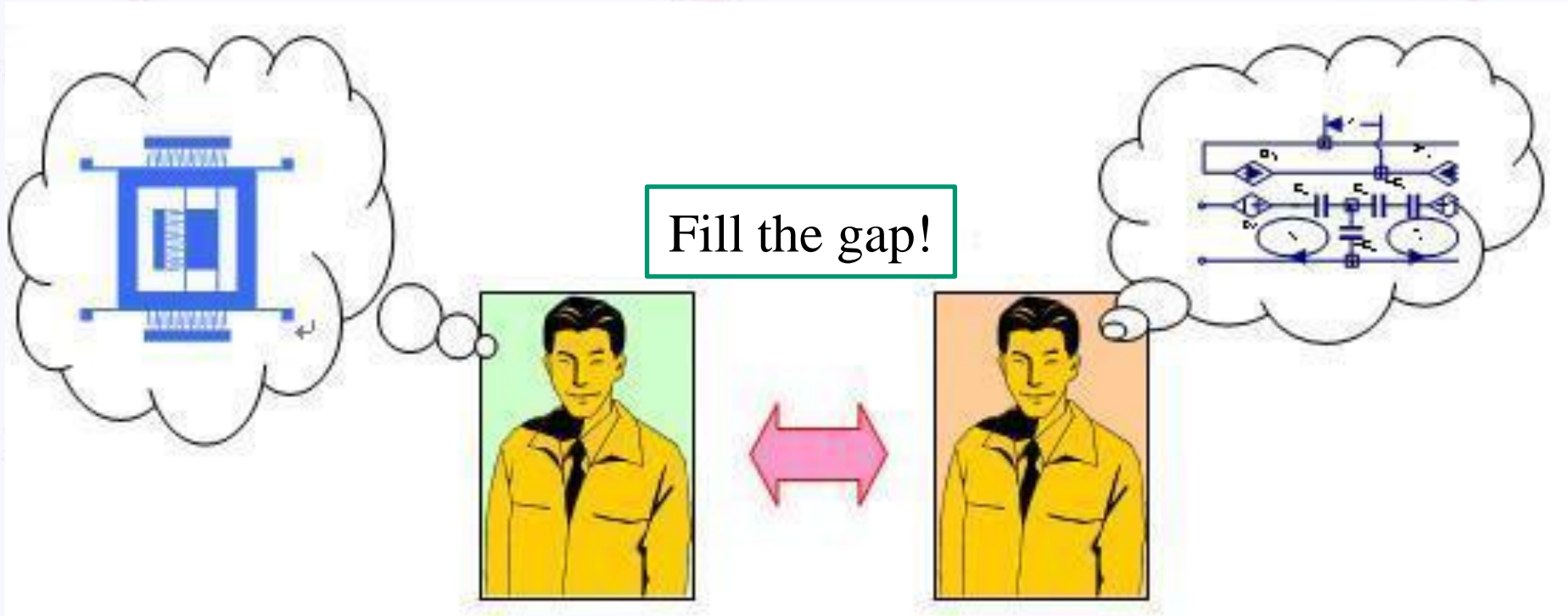
# Hierarchical integration of design & fabrication steps for CMOS-MEMS technology





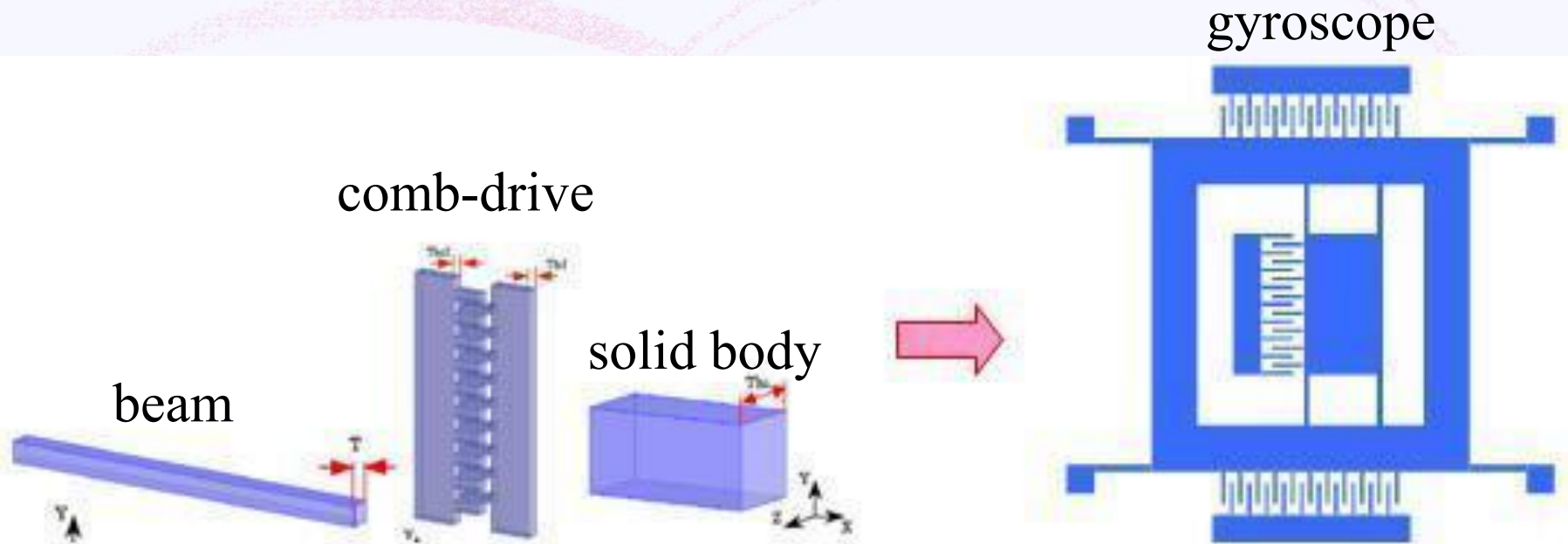
# MEMS equivalent circuit model generator

<http://memspedia.mmc.or.jp/WebLibrarySystem/>



Useful to fill the gap between MEMS engineers and VLSI engineers

# MEMS equivalent circuit model generator



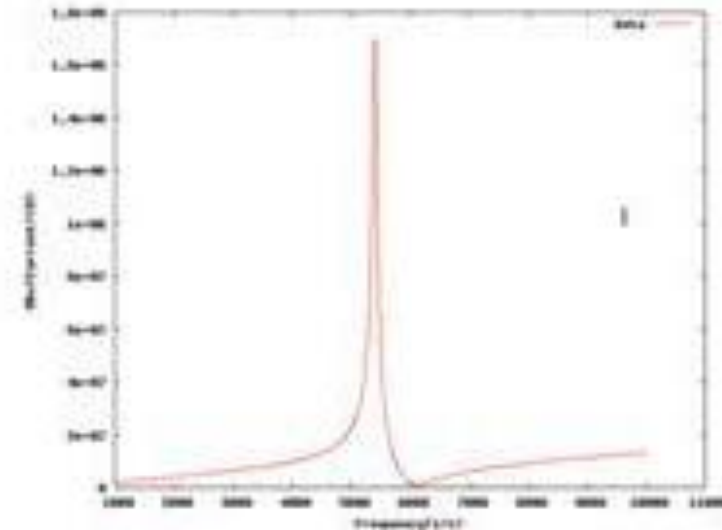
Connect basic components and construct a device  
 beam + comb-drive + solid body = gyroscope

# MEMS equivalent circuit model generator

Define connections



Simulated output



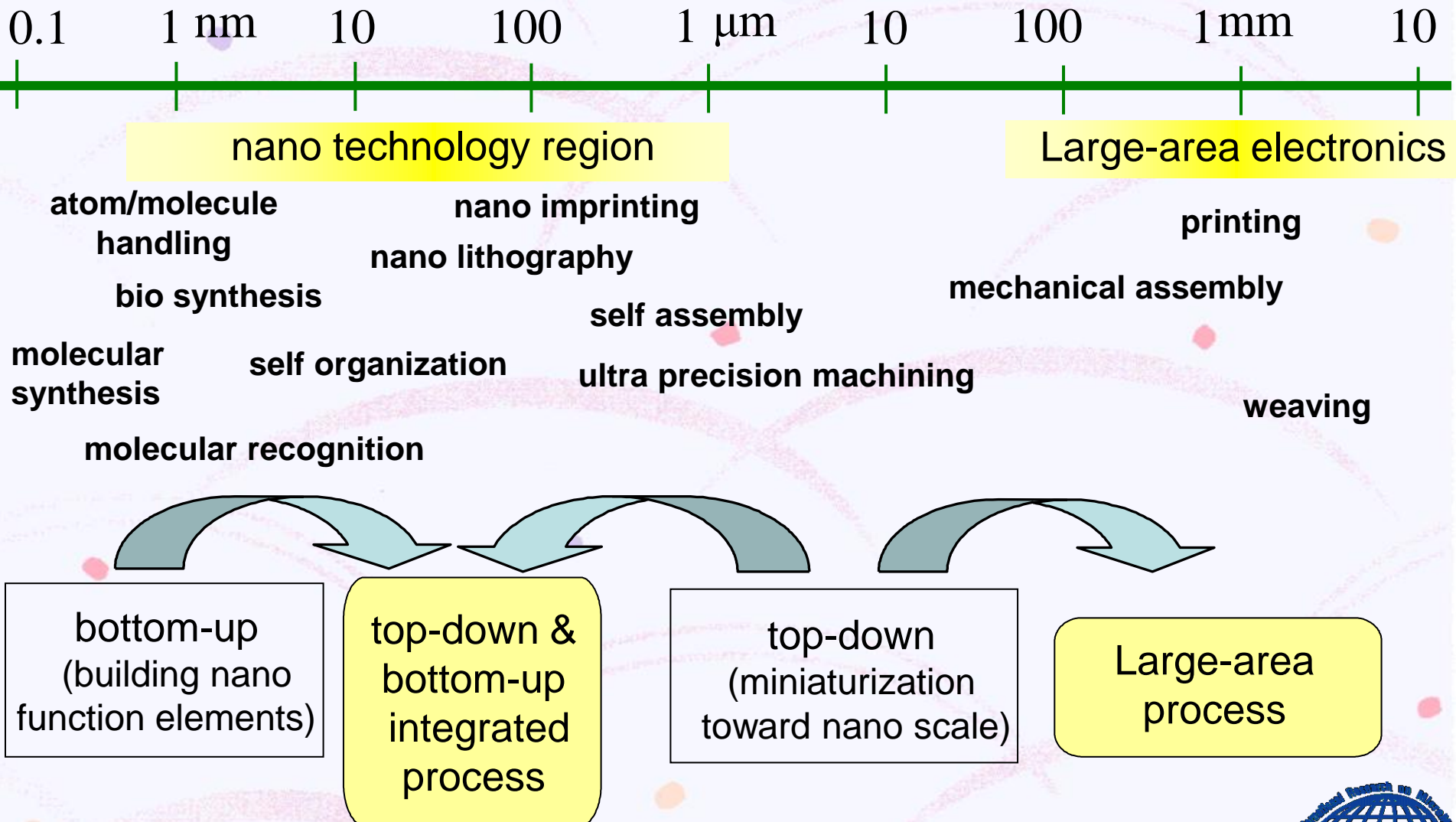
Each element is represented by an equivalent circuit. Connect them with external electrical circuit and perform SPICE simulation.

# Content

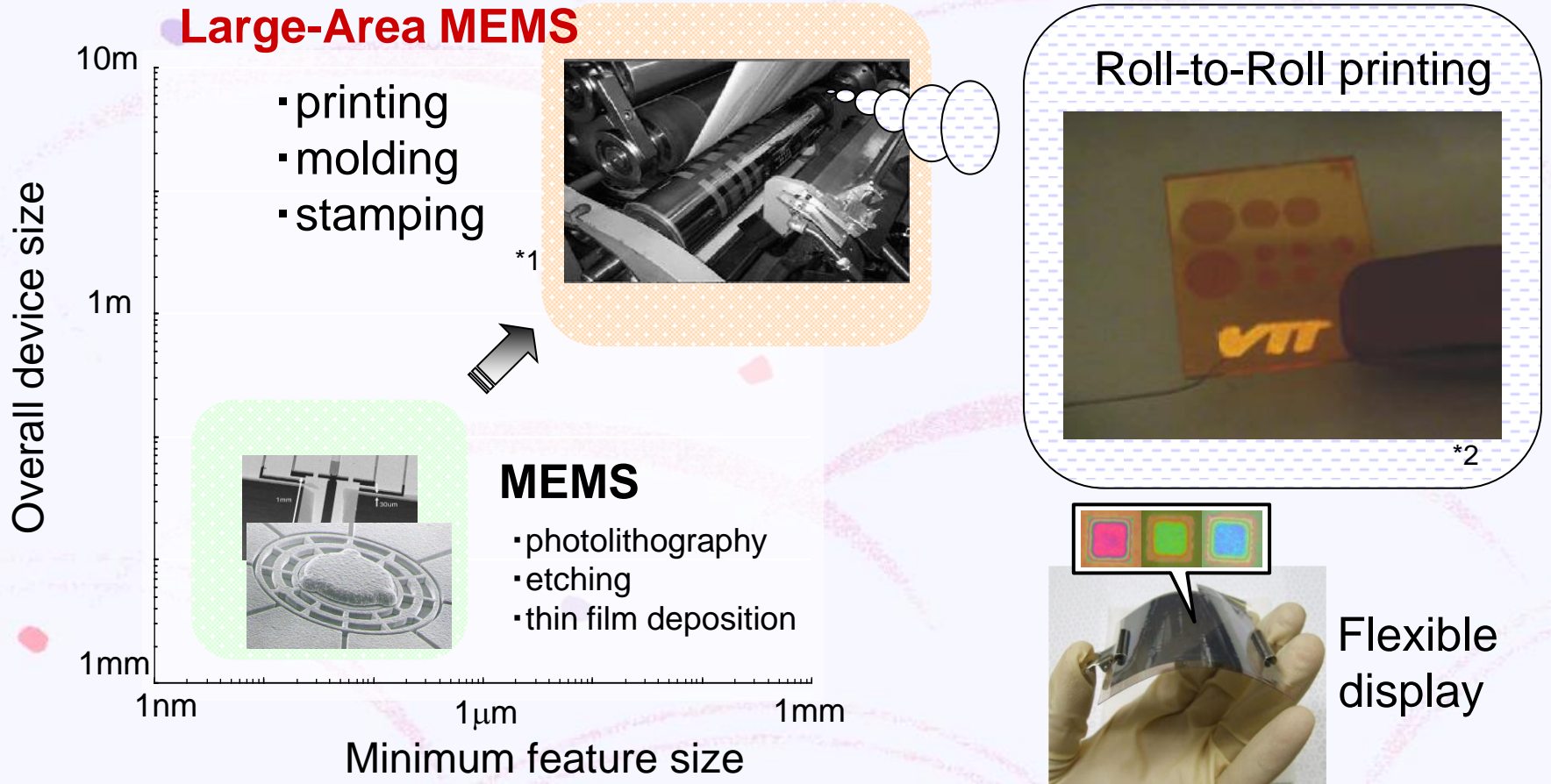
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# Process integration over the scale



# Large-Area MEMS



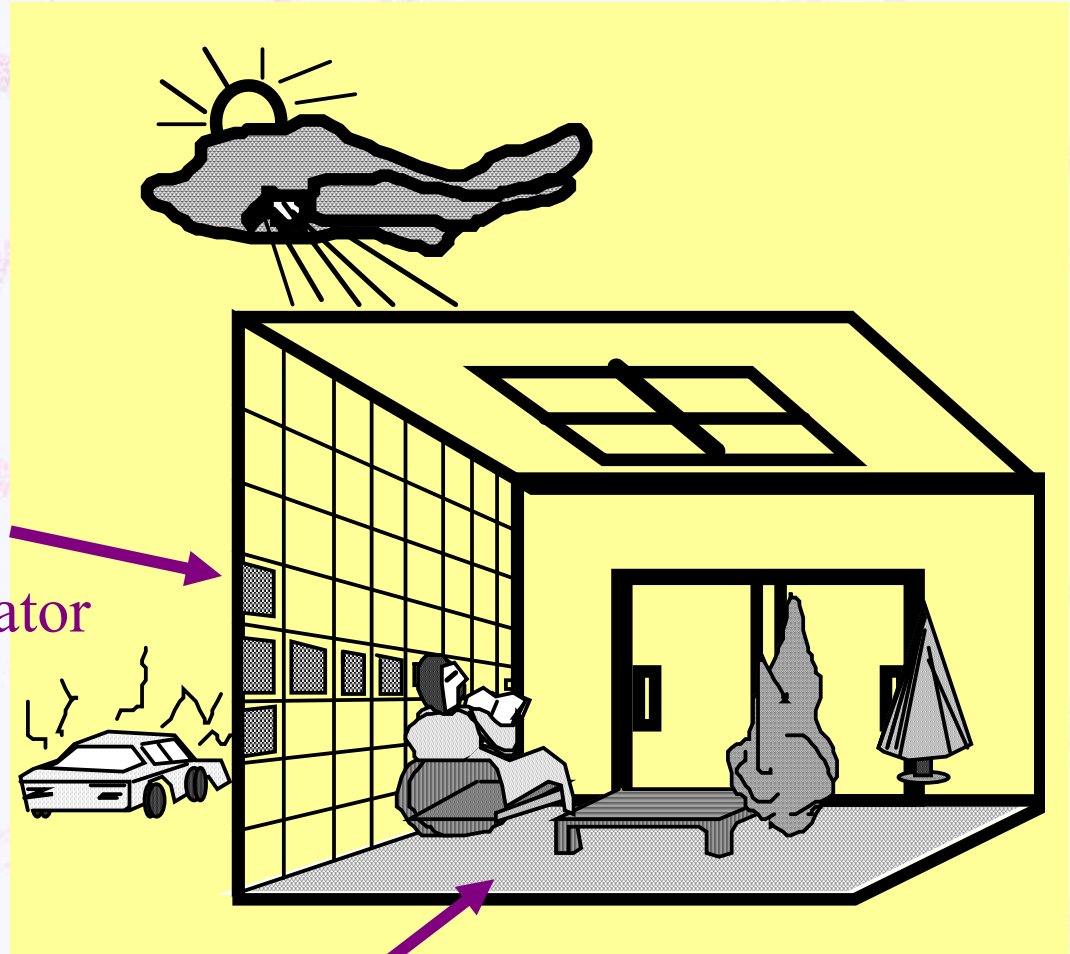
\*1 : Mäkelä, Tapio; Jussila, Salme; Vilkmán, M.; Kosonen, Harri; Korhonen, R. "Roll-to-roll method for producing polyaniline patterns on paper", Synthetic Metals. Vol. 135-136 (2003), 41-42

\*2 : <http://www.vtt.fi/>

# Smart-skin wall paper and carpets

Room environment is kept comfortable by arrayed MEMS sensors and actuators.

Optical sensor + LED  
 Microphone + speaker  
 Temp. sensor + heater  
 Humidity sensor + ventilator  
 Human sensor  
 on wall paper & carpet

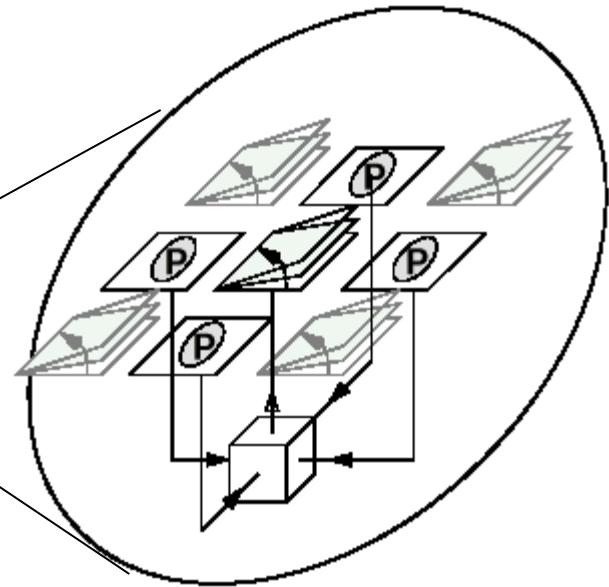
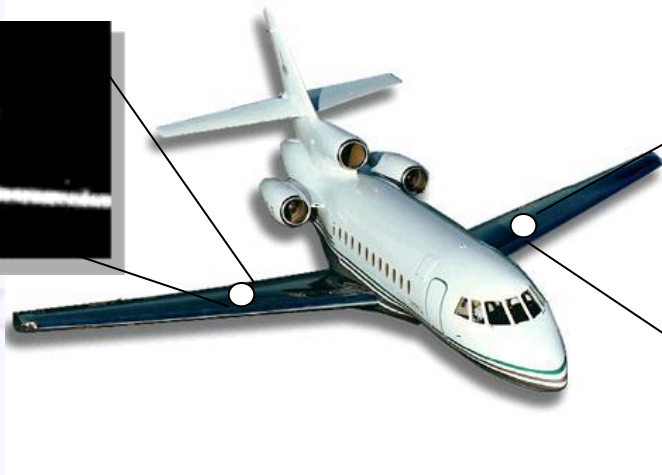


Active MEMS carpet for cleaning

# Smart skin (intelligent surface)

- Taking best advantages of MEMS features  
**3M** : Miniaturization , Multiple , Microelectronics

## Adaptative Wing

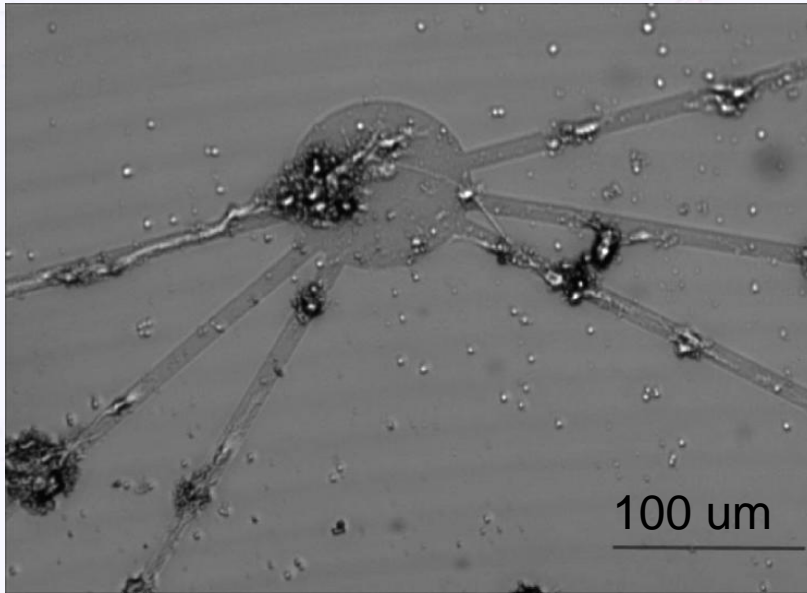


Sensors + Local data processing + Actuators

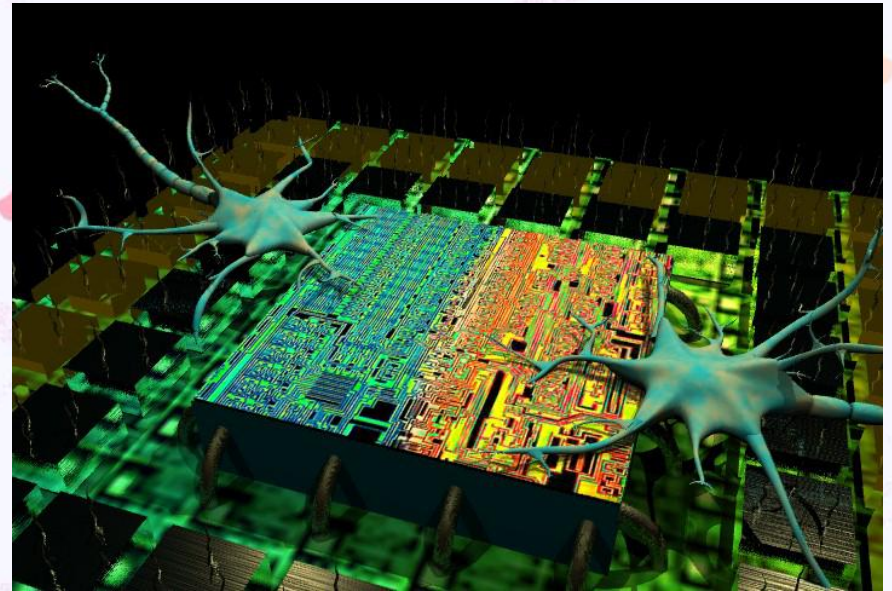


# MEMS guided axon for BMI

4-dimensional micromachining including temporal development



Cultured neuron cells elongate axons along micro patterns on a chip



Prospected BMI

# Future trends

- Micro/nano machining technology in the future must be the **integration of top-down methods** (such as MEMS or VLSI) and **bottom-up methods** (such as molecular synthesis and bio technology).
- **Autonomous MEMS instruments** to capture ambient information will be important for security, personal health care, and environmental protection. Wireless devices and the MEMS energy source will play key role.
- New fabrication technology for **large area integration** of various functional devices will be important. Such products as flexible/interactive display, MEMS wall paper for lighting/air-conditioning/noise-reduction, and smart clothes may be produced.

# Conclusion

- MEMS Technology has matured and ready for CMOS-MEMS integration: *More-than-Moore*
- Four ways to integrate MEMS and CMOS. Hybrid integration is most practical. Fully mixed process and MEMS-first process are suitable to mass production of many devices. CMOS-first process is flexible and compatible with existing foundry system.
- Beyond CMOS-MEMS integration, bio/nano objects will be integrated on chip. Also process for smart skin will be required.

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